

Prom Name	Rev	Part No.	Location	Page	Comments
SwitchProm	R	F93427	i14	14	New Rev for 16K Control Store CP 256 x 4
KernPC16Prom	B	F93427	h14	15	Standard 256 x 4
CSIntProm	D	F93453	e20	22	Standard 1K x 4
StackVirtProm	I	F93427	h24	15	Standard 256 x 4
ScheduleProm	D	F93453	h18	14	Standard 1K x 4
ErrorProm	E	F93453	g14	15	Standard 1K x 4
IBProm-PC.0	G	F93453	i17	05	Standard 1K x 4
IBProm-PC.4	G	F93453	h17	05	Standard 1K x 4
DesMpProm.0	B	F93427	a16	33	Added to control DES logic 256 x 4
DesMpProm.4	B	F93427	b16	33	Added to control DES logic 256 x 4
DesSpProm	A	F93427	b15	33	Added to control DES logic 256 x 4

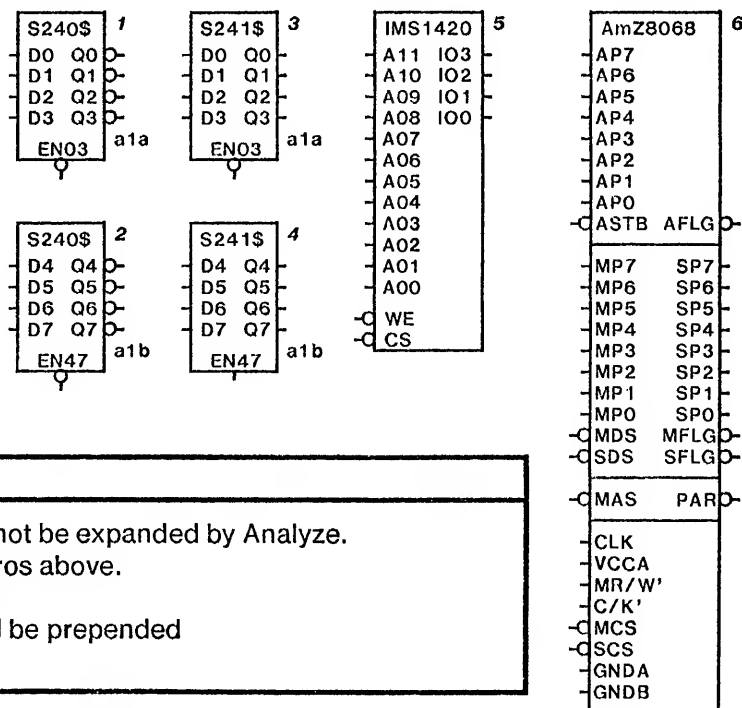
Prom files are stored on [Indigo]<Dandelion>CPE>Proms>\*

Bringover /a [Indigo]<Dandelion>CPE>DfFiles>Proms.df to fetch all files, sources, tools, etc.

#### Labels:

Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A

#### Font 4 Macros



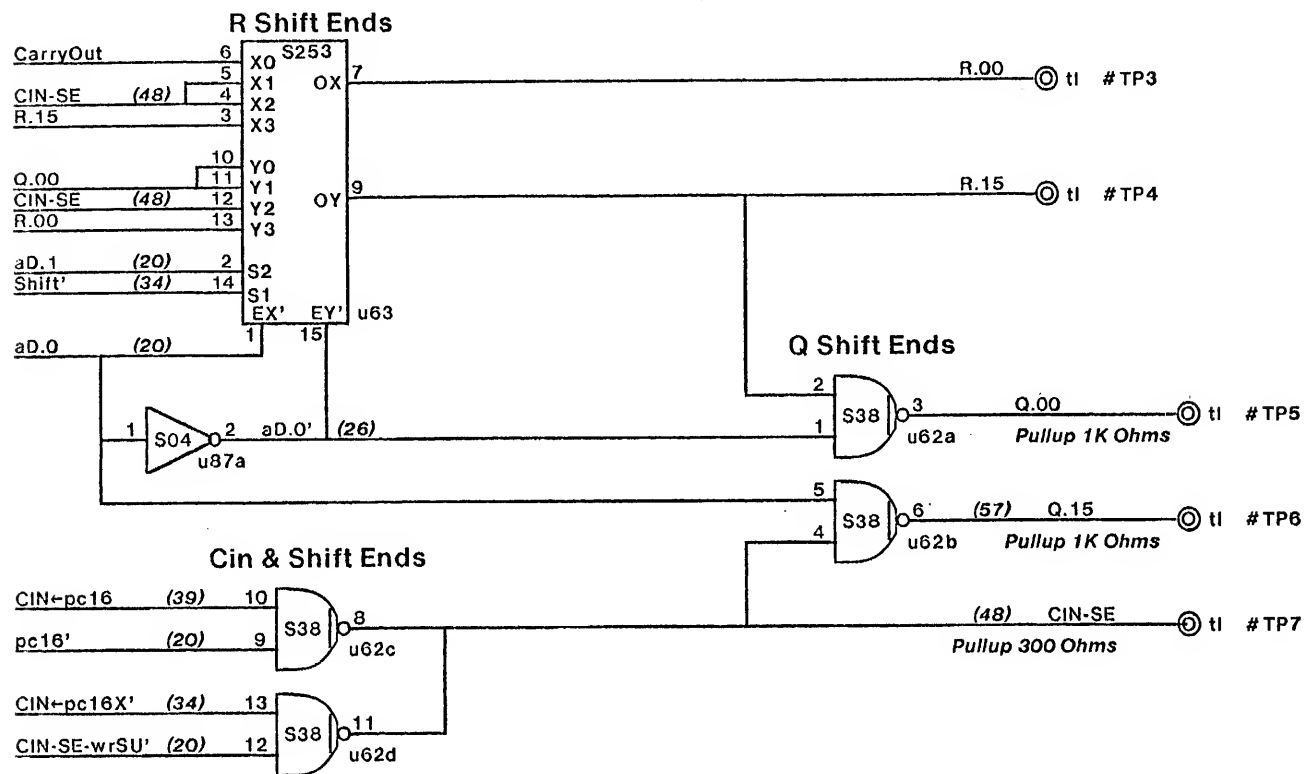
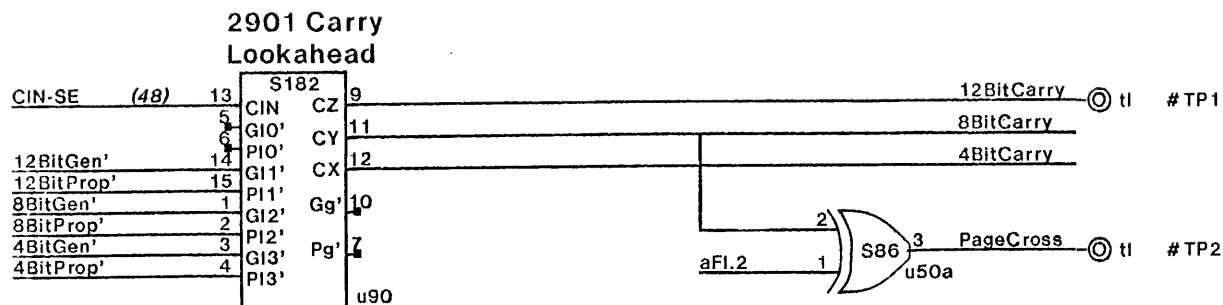
#### Important Notes:

Only macros 0-9 are valid component names and will not be expanded by Analyze.  
Some of these drawings contain instances of the macros above.  
Those that do have a warning on them, see below left.  
There is a corresponding CPEDict.analyze that should be prepended  
to the dictionary chain.

Warning: This drawing contains font 4 macros!

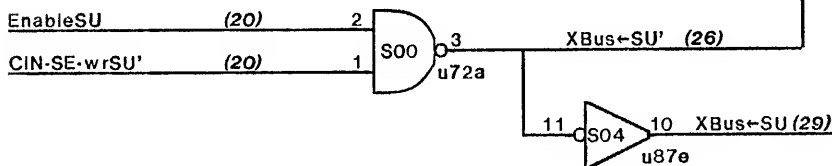
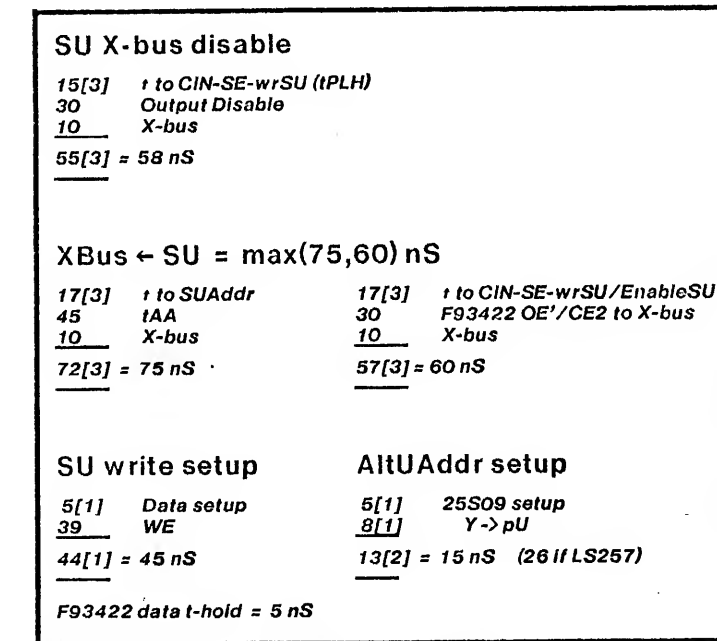
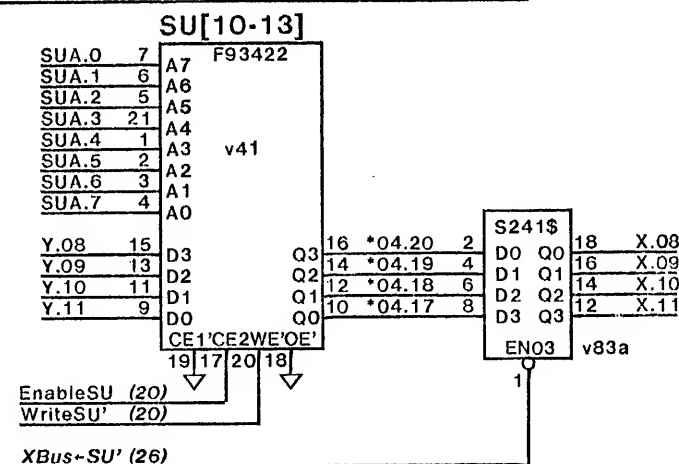
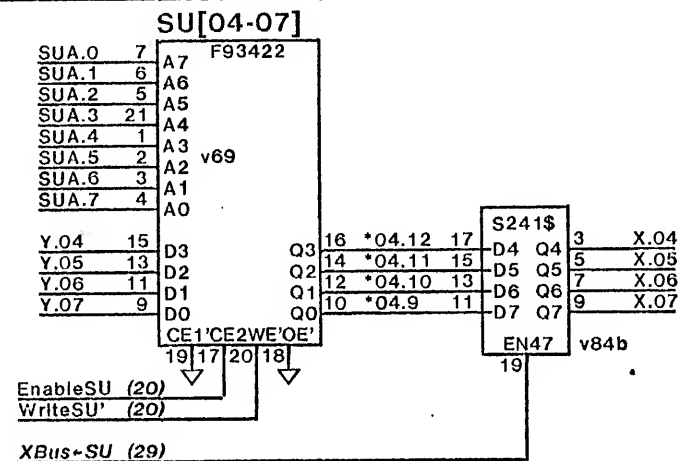
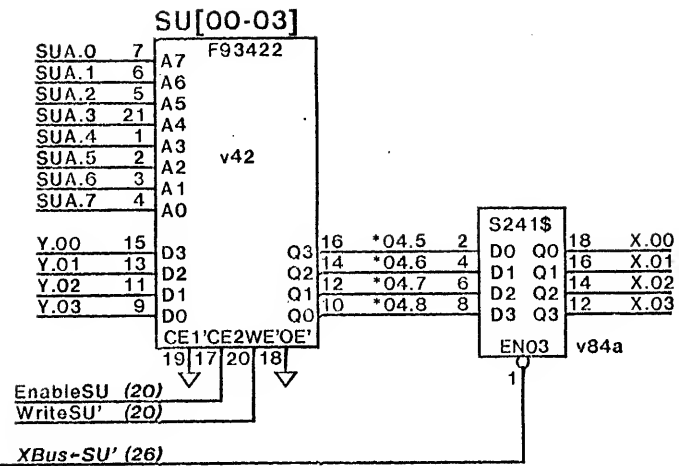
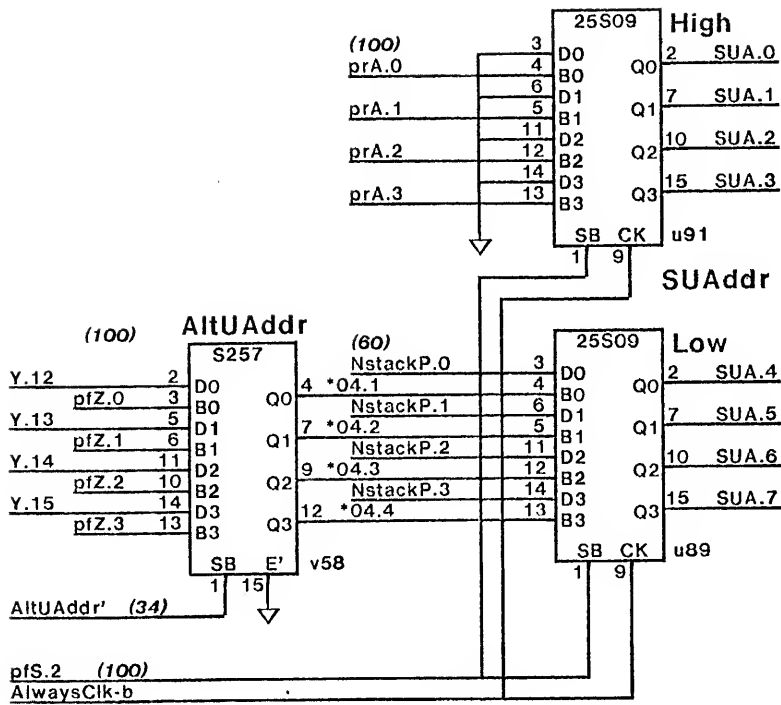
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P12560		SHEET REV. A
	TITLE SCHEMATIC, CPE-FP <div>Reference</div>			SHEET 02 OF		



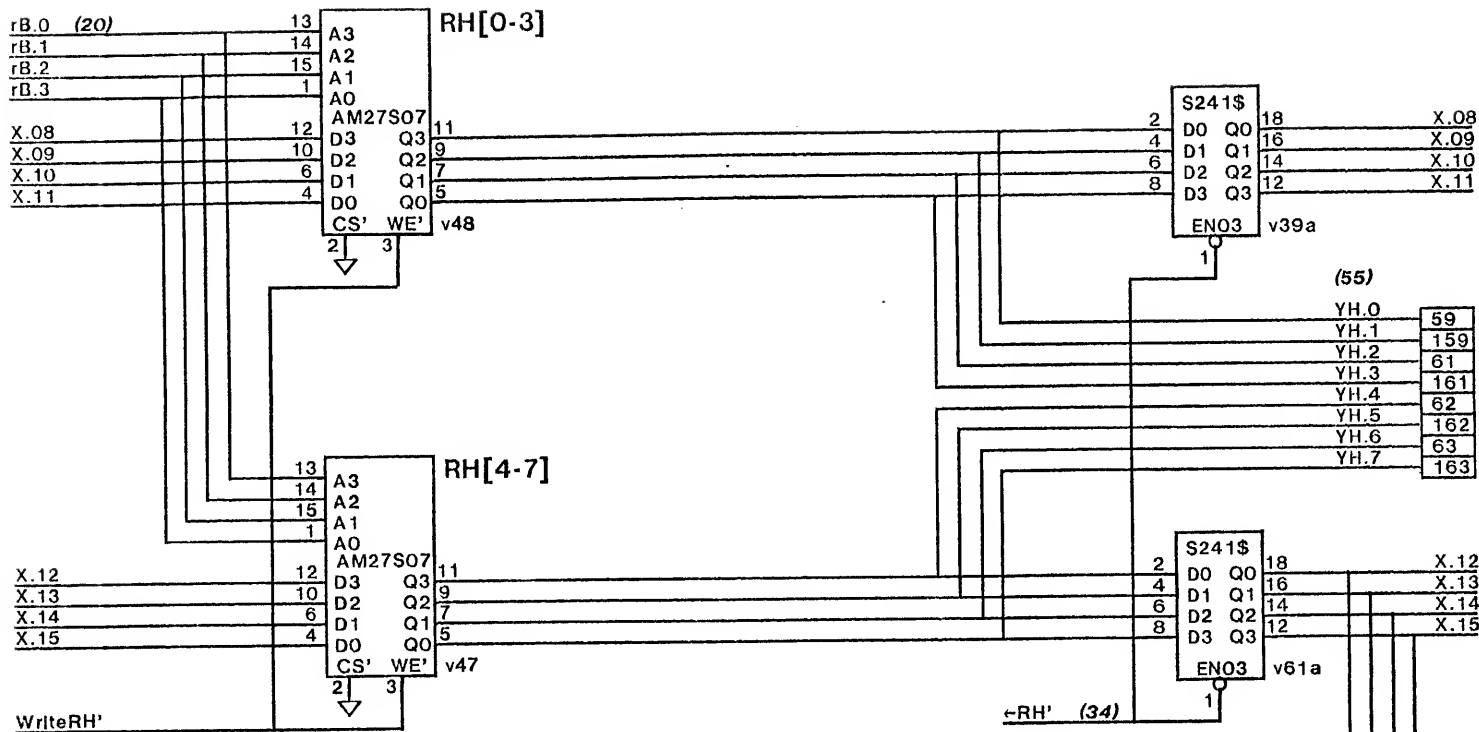


aD.1	Shift'	Shift configuration
0	0	
0	1	
1	0	
1	1	

aD.0 = 0 implies right shift



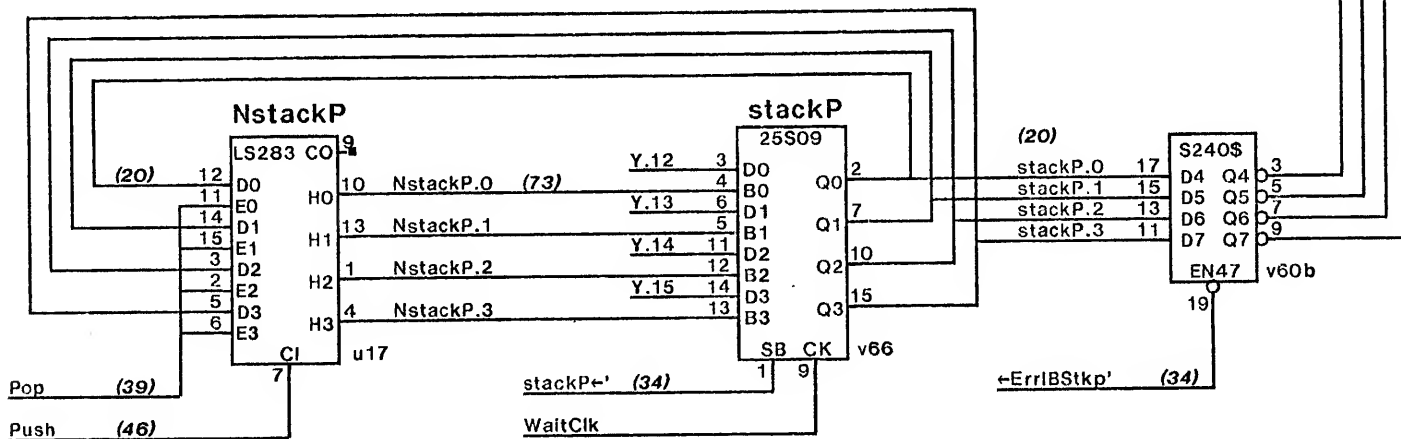
Warning: This drawing contains font 4 macros!



**XBus  $\leftarrow$  RH = max(74,59) nS**

**Timing Parameters:**

- $17[3]$   $t$  to  $rB'$
- $35$   $S189$   $t_{AA}$  ( $wr$  recovery = 35 nS)
- $9$   $YH$  to  $X$
- $10$   $X$ -bus
- $71[3] = 74$  nS
- $34$   $t$  to  $-RH'$
- $15$   $S241$   $EN'$  to  $X$ -bus
- $10$   $X$ -bus
- $59$  nS



**Push Timing**

**Timing Parameters:**

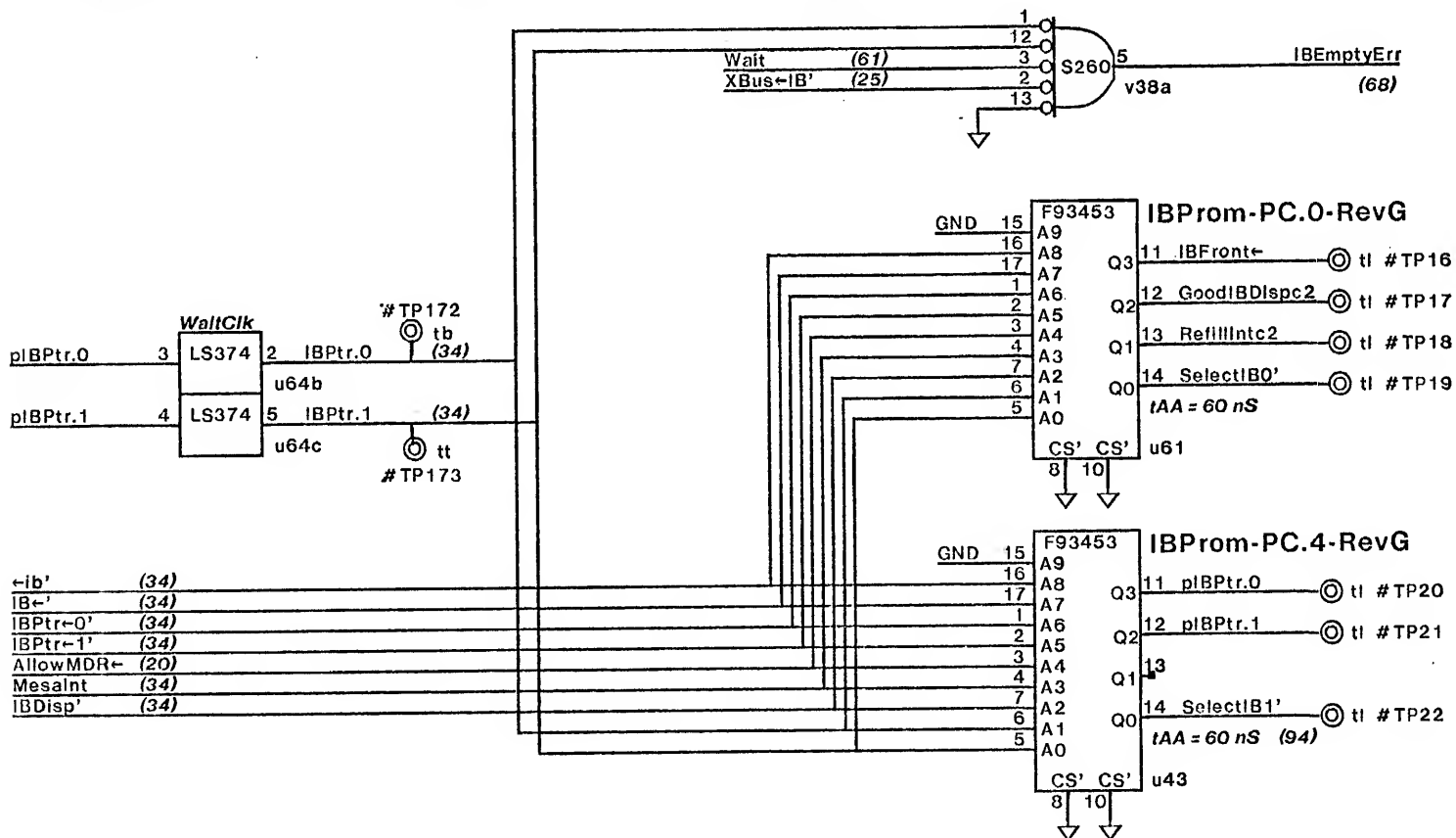
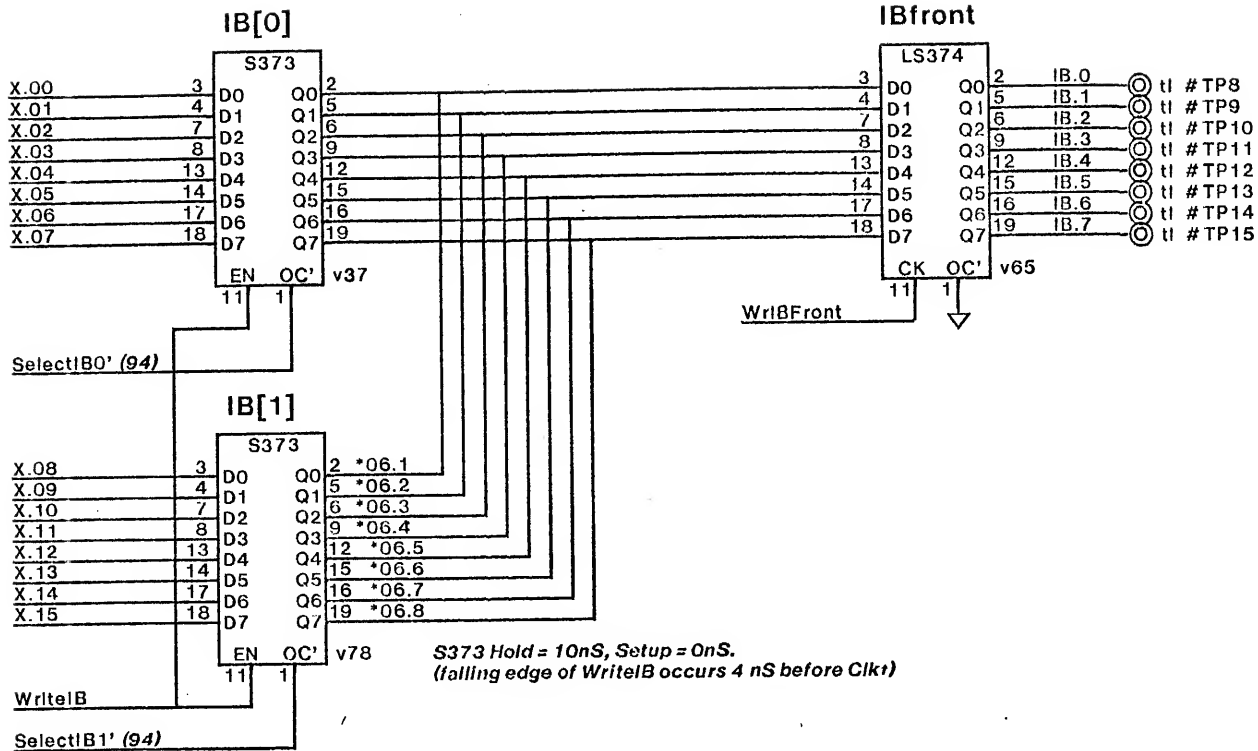
- $46$   $t$  to  $Push$
- $24[3]$   $Push$  to  $NstackP$
- $5[1]$   $25S09$  setup
- $75[4] = 79$  nS

**XBus  $\leftarrow$  stackP = max(59, 38) nS**

**Timing Parameters:**

- $17[3]$   $t$  to  $stackP$
- $7$   $S240$  data to  $X$ -bus
- $10$   $X$ -bus
- $34[3] = 38$  nS
- $34$   $t$  to  $-ErrIntstackP'$
- $15$   $S240$   $EN'$  to  $X$ -bus
- $10$   $X$ -bus
- $59$  nS

Warning: This drawing contains font 4 macros!



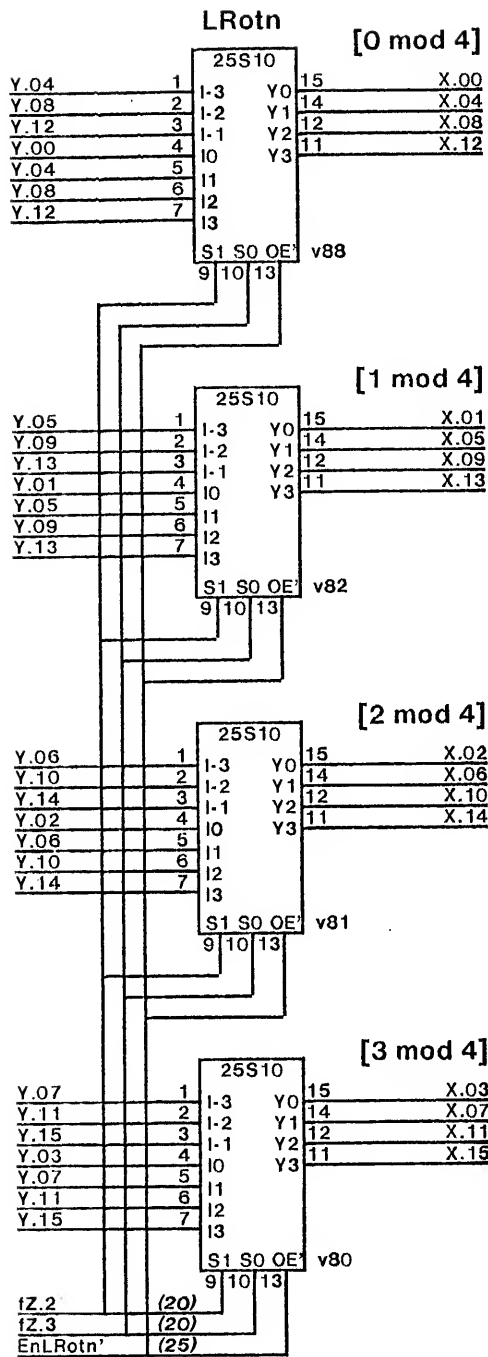
# Timing for HM7649 IBProm

(Old Proms -- not 2nd sourced)

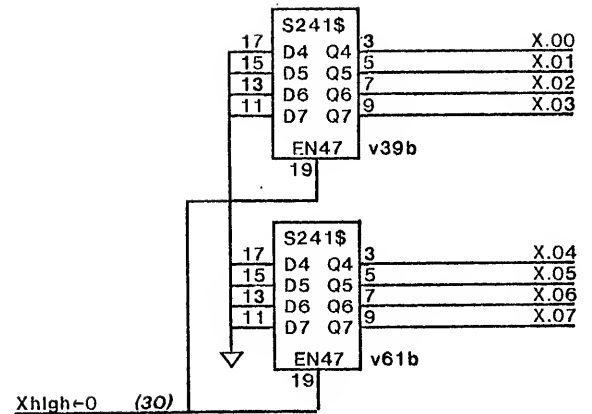
IBfront ← Xbus = (x + 37, x + 36) nS

x	Xbus to IB	x	Xbus to IB	94	WritelB rises	34	t to IBPtr-1'
43	WritelB rises 43 nS before end of cycle	13[1]	S373 Data to NB	18[2]	S373 EN to NB	60	tAA
-6	Difference between S373 "EN to Q" and "Data to Q" =	20[2]	LS374 setup	20[2]	LS374 setup	18[2]	SelectIB1' to NB
x + 37 nS	18[2] - 13[1] = 6 nS. Data can arrive 6 nS after WritelB goes high.	x + 36 nS		132[4] = 136 nS		20[2]	LS374 setup
						132[4] = 136 nS	

IBfront ← IB[1]



fZ.2	fZ.3	Rotate
0	0	Left 0
0	1	Left 12
1	0	Left 8
1	1	Left 4



#### Zero disable X-bus

30  $t$  to Xhigh=0  
 15 S241 EN to X-bus  
 10 X-bus  
 55 nS

#### Xbus[0-7] ← 0

30  $t$  to Xhigh=0  
 15 S241 OE  
 10 X-bus  
 55 nS

#### Xbus ← Y LRotn = max(y + 22, 56, 50) nS

y  $t$  to Y bus  
 12 25S10 data in to out  
 10 X-bus  
 y + 22 nS

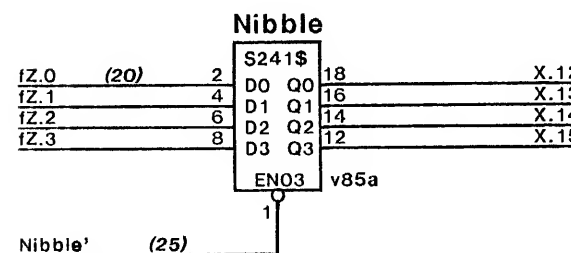
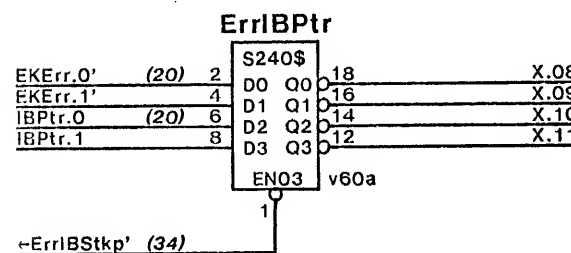
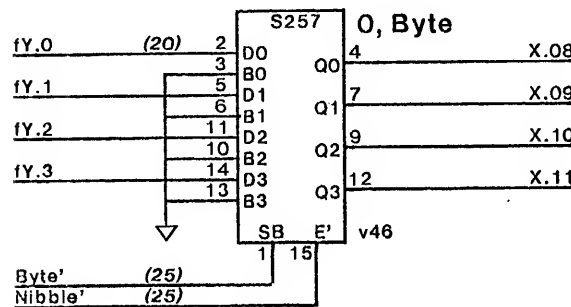
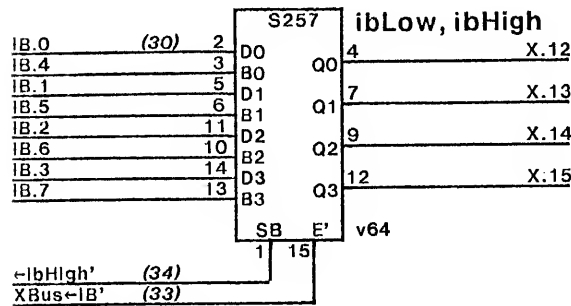
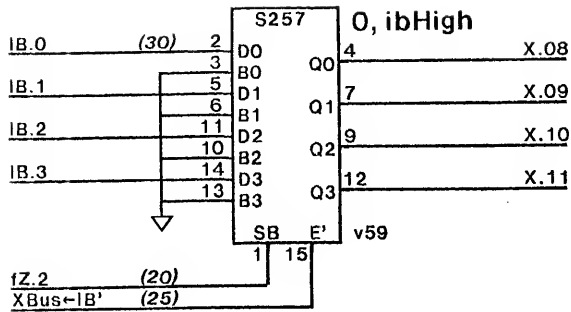
25  $t$  to EnLRotn'  
 21 25S10 OE  
 10 X-bus  
 56 nS

20  $t$  to fZ.2  
 20 25S10 Select to X-bus  
 10 X-bus  
 50 nS

#### LRotn disable X-bus

25  $t$  to EnLRotn'  
 15 25S10 OE' to X-bus  
 10 X-bus  
 50 nS

Warning: This drawing contains font 4 macros!



### IB disable X-bus

25 t to XBus-IB'  
14 S257 E' to X-bus  
10 X-bus  
49 nS

### Byte disable X-bus

25 t to Nibble'  
14 S257 E' to X-bus  
10 X-bus  
49 nS

### Nibble disable X-bus

25 t to Nibble'  
15 S241 EN' to X-bus  
10 X-bus  
50 nS

### Xbus<-IB = max(56,56,59) nS

34[4] t to IB  
8 S257 data to Xbus  
10 X-bus  
52[4] = 56 nS  
25 t to Xbus-IB'  
21 S257 E' to Xbus  
10 X-bus  
56 nS  
34 t to-ibHigh'  
15 S257 SB to Xbus  
10 X-bus  
59 nS

### Xbus <- Nibble = max(39, 50) nS

20 t to fZ  
9 S241 data to X-bus  
10 X-bus  
39 nS  
25 t to Nibble'  
15 S241 EN' to X-bus  
10 X-bus  
50 nS

### Xbus <- Byte = max(38, 56,50) nS

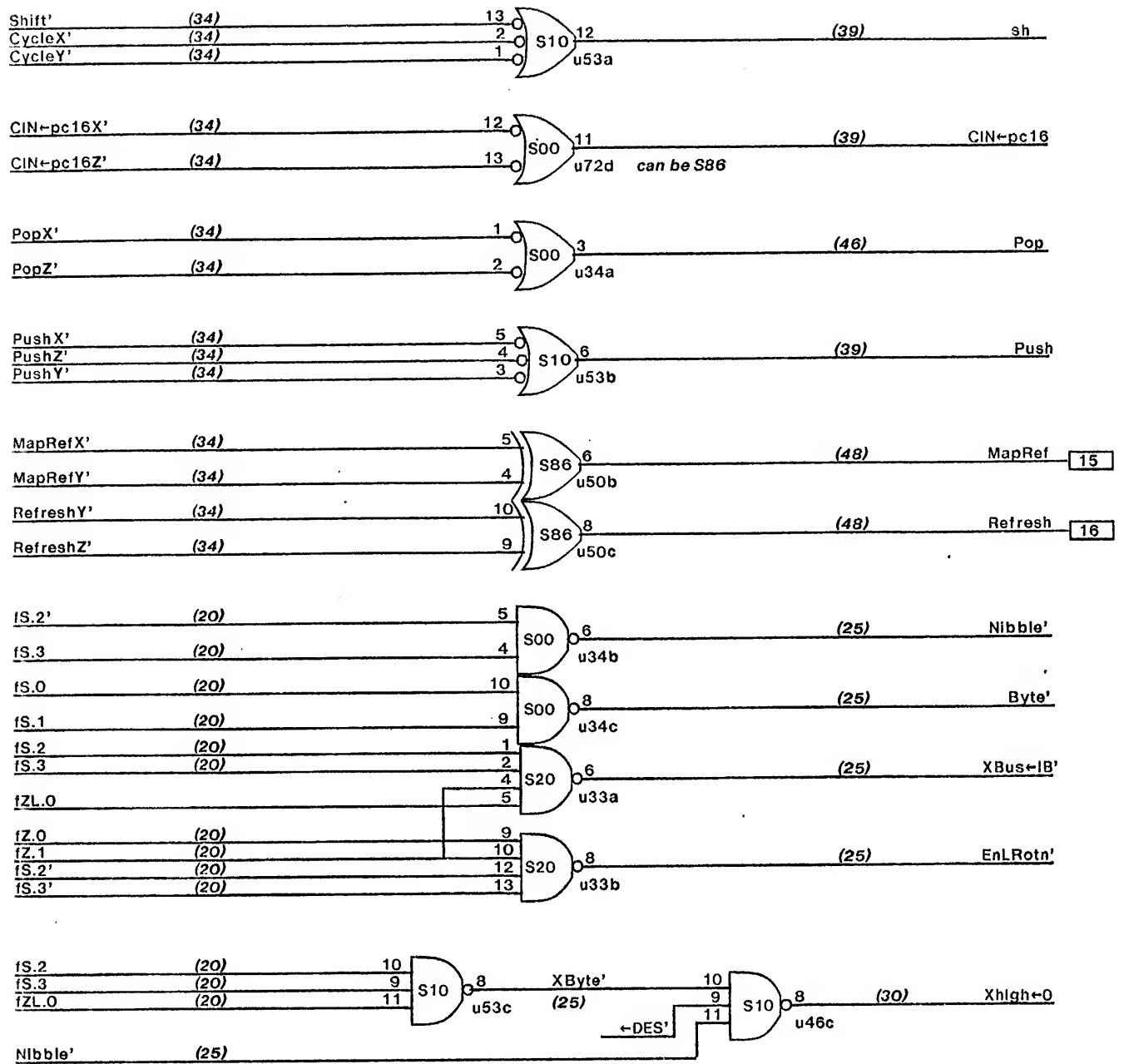
20 t to fY  
8 S257 data to X-bus  
10 X-bus  
38 nS  
25 t to Nibble'  
21 S257 E' to X-bus  
10 X-bus  
56 nS  
25 t to Byte'  
15 S257 SB to Xbus  
10 X-bus  
50 nS

See stackP timings for ErrIBPtr

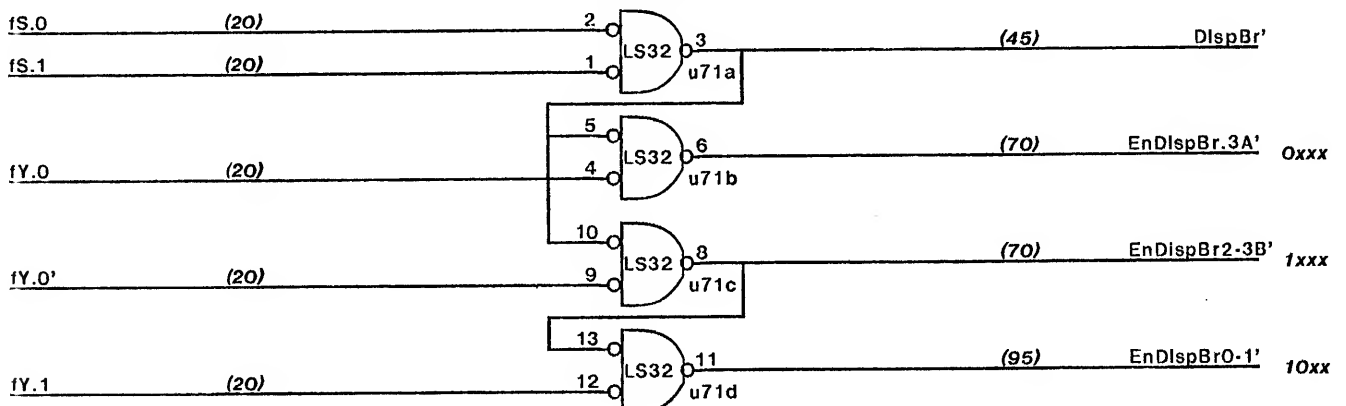
Warning: This drawing contains font 4 macros!

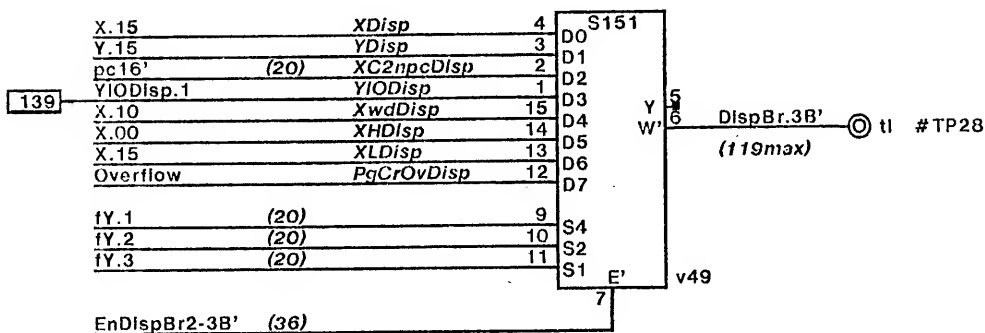
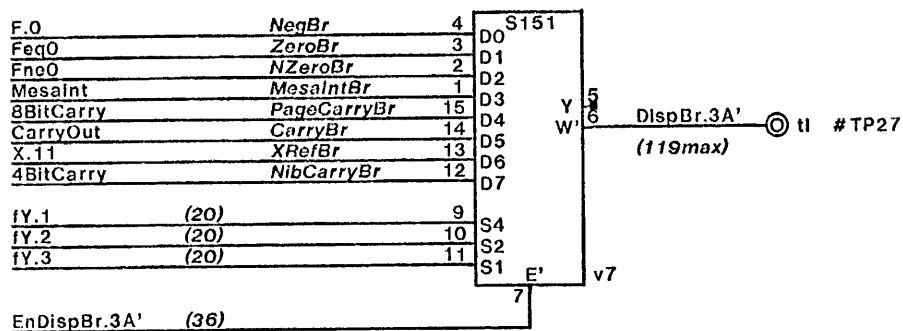
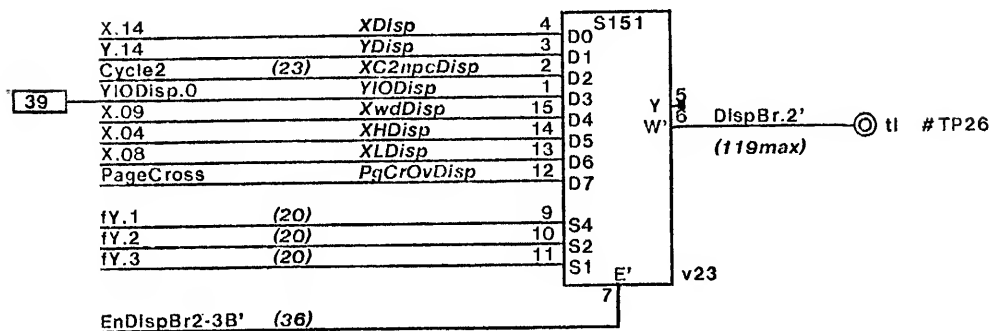
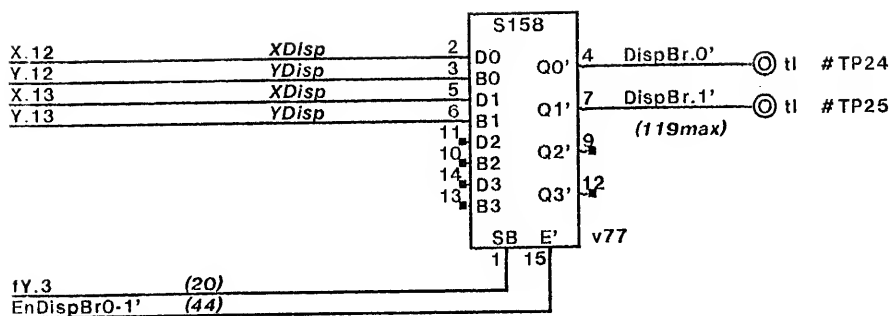






### EnDispBr





DispBr[0-1] = max(c + 32, 69, 133)

20 t to fY  
24[3] S151 select to DispBr  
18 DispBr' setup  
64[3] = 69

95 t to EnDispBr0-1'  
18[2] S151 E' to DispBr  
18 DispBr' setup  
131[2] = 133 nS

c condition source  
12[2] S151 data to DispBr  
18 DispBr' setup  
c + 30[2] = c + 32

### DispBr Setup

5 S00 In to pTC  
6[1] S64 In to pNIA  
5[1] 25S09/S374 setup  
18 nS

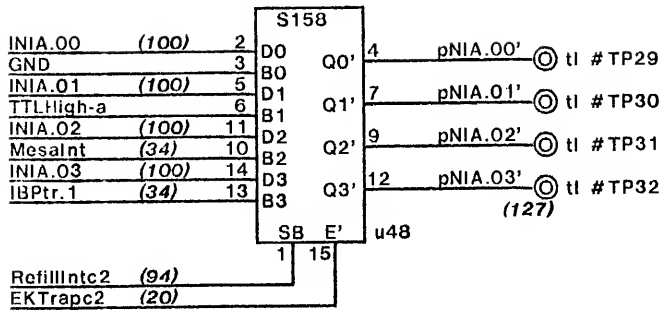
DispBr[2-3] = max(c + 26, 55, 103)

20 t to fY  
15[2] S151 select to DispBr  
18 DispBr' setup  
51[4] = 55 nS

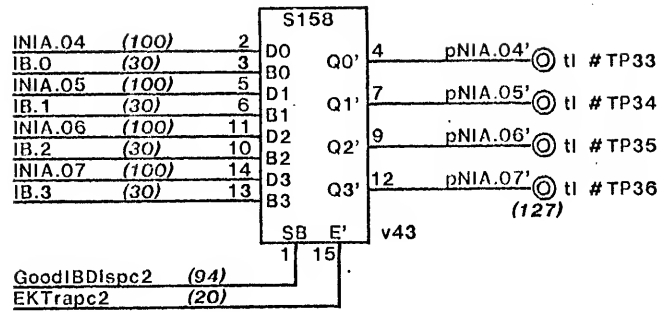
70 t to EnDispBr.3A'  
13[2] S151 E' to DispBr  
18 DispBr' setup  
101[2] = 103 nS

c condition source  
7[1] S151 data to DispBr  
18 DispBr' setup  
c + 23[3] = c + 26 nS

### pNIA[0-3]



### pNIA[4-7]



$$pNIA[0-7] = \max(127, 120, 46) \text{ nS}$$

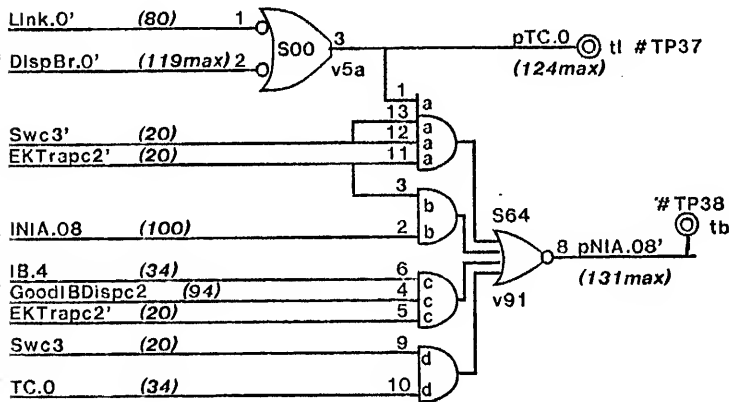
94  $t$  to RefillIntc2  
24[3] LS158 SB to pNIA'  
5[1] 25S09/S374 setup  
123[4] = 127 nS

100  $t$  to INIA  
12[2] LS158 data to pNIA'  
5[1] 25S09/S374 setup  
117[3] = 120 nS

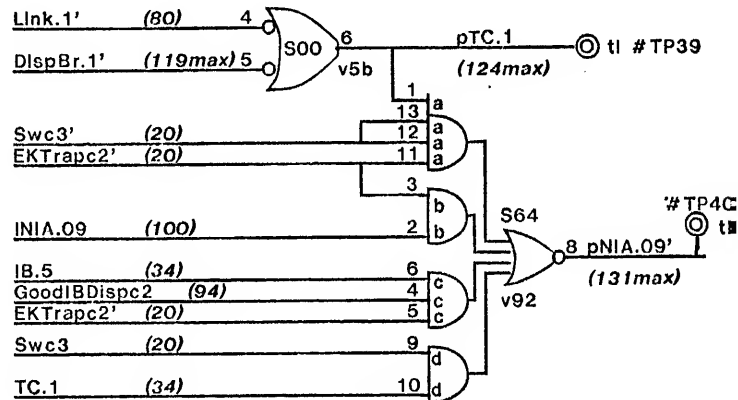
20  $t$  to EKErrc2  
18[2] LS158 E' to pNIA'  
5[1] 25S09/S374 setup  
43[3] = 46 nS

(See page 11 for pNIA[8-11] timing)

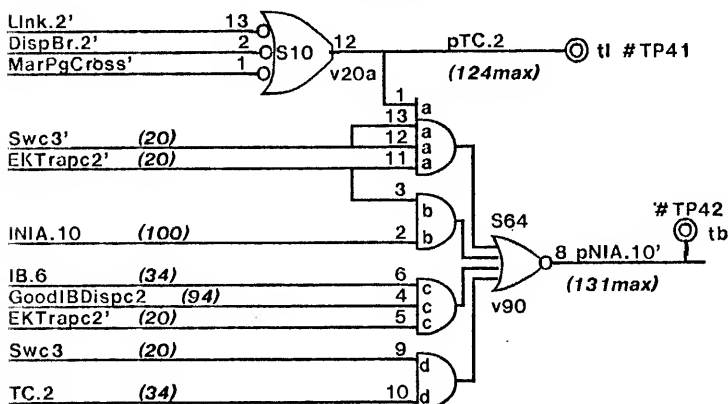
### pNIA.8



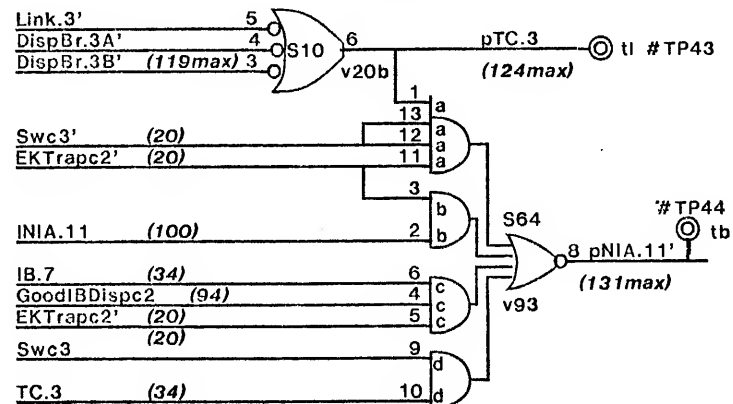
### pNIA.9



### pNIA.10



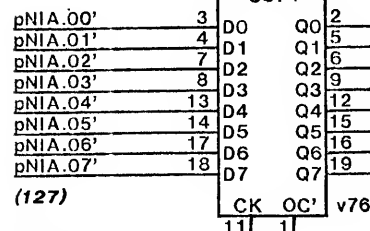
### pNIA.11



NIA X.00' (20) From IOP Receivers, Page 20

NIA X.01'  
NIA X.02'  
NIA X.03'  
NIA X.04'  
NIA X.05'  
NIA X.06'  
NIA X.07'  
NIA X.08'  
NIA X.09'  
NIA X.10'  
NIA X.11'

NIA X[00-07]



AlwaysClk-c  
SwTAddr (20)

Nt.0 (77)  
Nt.1  
Nt.2

### Link timing

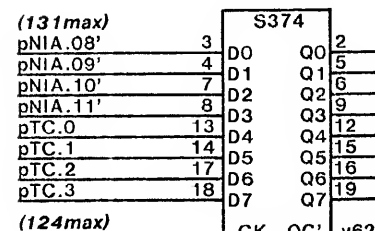
20  $t$  to fX  
35 Am27S07 tAA  
22[3] pLink' to Link'  
18 DispBr' setup

95[3] = 98 nS

20  $t$  to fX.0, NIA X.7'  
22[3] fX.0 to pRet'  
22[3] pRet' to Link'  
18 DispBr' setup

82[6] = 88 nS

NIA X[08-11]



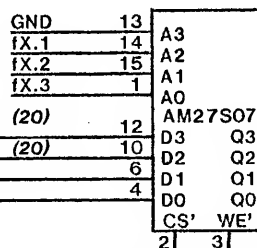
(124max)  
AlwaysClk-c  
SwTAddr (20)

If only pullups were used  
on output of Link (instead  
of the LS32 kludge), then  
Link timing would be:

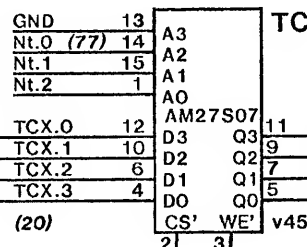
98 WriteLink' active  
25[3] WE' to pLink high  
18 DispBr' setup  
141[3] = 144 nS

### TPC/TC timing

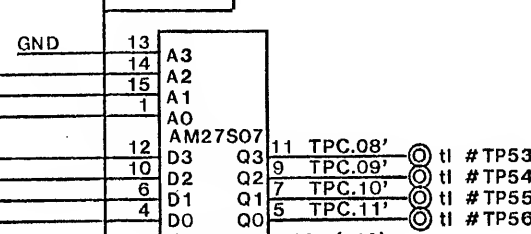
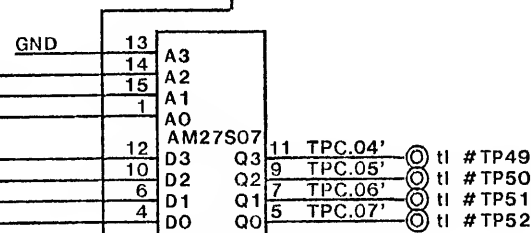
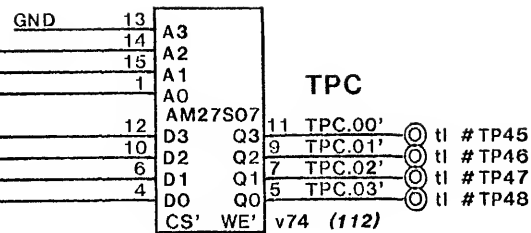
77  $t$  to Nt  
35 Am27S07 tAA  
5[1] 25S09/S374 setup  
117[1] = 118 nS



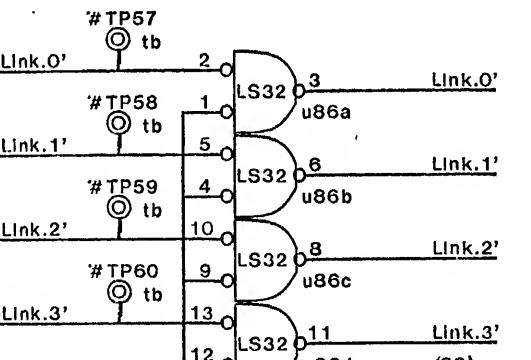
fX.0 (20)  
WriteLink'  
NIA X.07' (20)



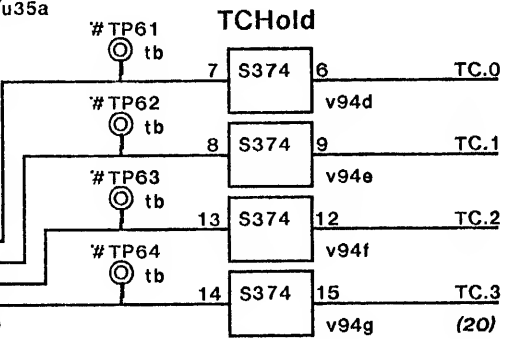
(20)  
WriteTC'



WriteTPC'

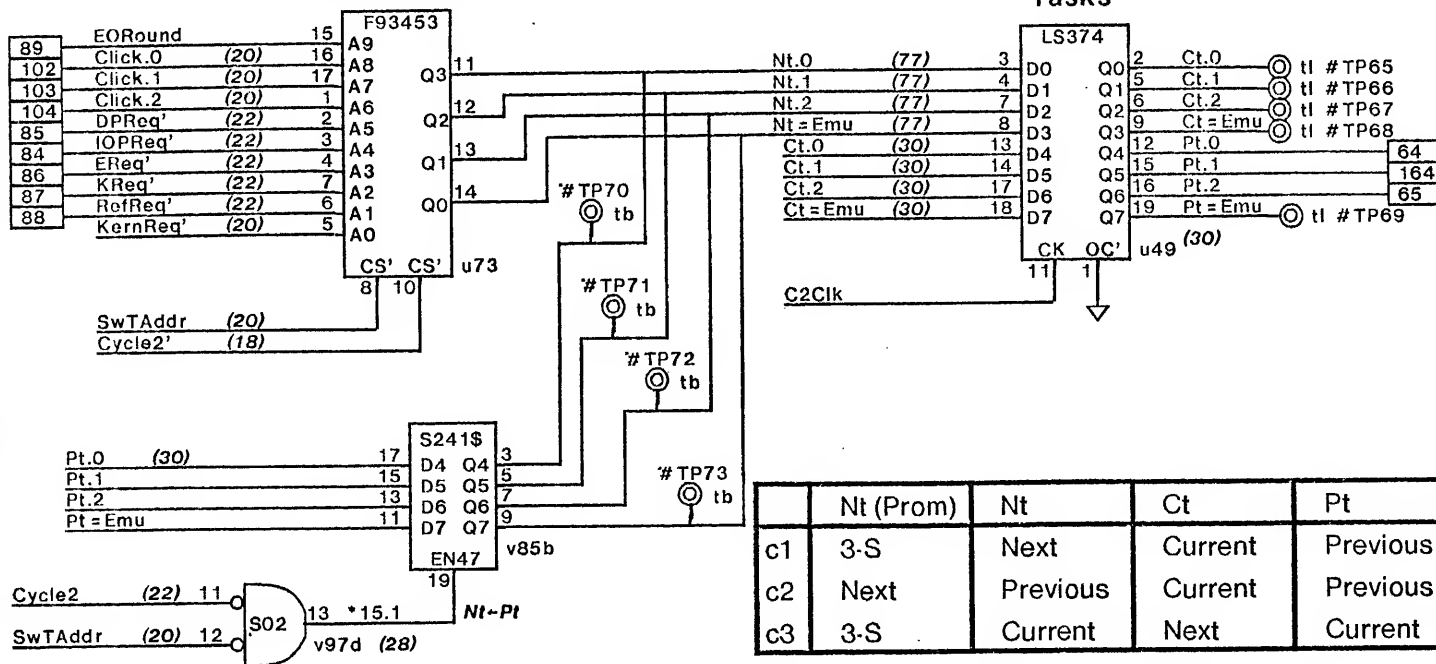


(80)

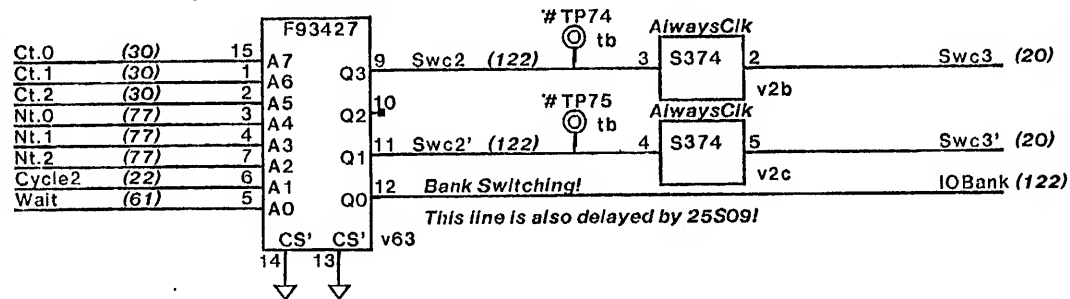


AlwaysClk

## ScheduleProm-RevD



## SwitchProm-RevR



Note: This is a non-standard PROM. IOBank has been added!

## Task Numbers

0	Emulator
1	Display/LSEP
2	Ethernet
3	Refresh
4	Disk
5	IOP
6	Control Store R/W
7	Kernel

Swc2 timing = max(133,101,101)

22	↑ to Kreq'	20	↑ to SwTAddr	28	↑ to Nt-Pt
55	F93453 addr to Nt	25	F93453 CS' to Nt	15[2]	S241 EN to Nt
45	F93427 addr to Swc2	45	F93427 addr to Swc2	45	F93427 addr to Swc2
10[1]	25S09 SB setup	10[1]	25S09 SB setup	10[1]	25S09 SB setup
132[1] = 133 nS		100[1] = 101 nS		98[3] = 101 nS	

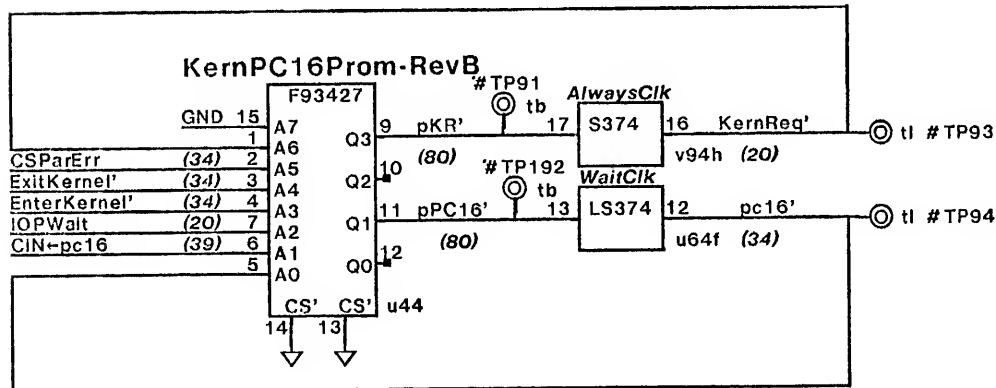
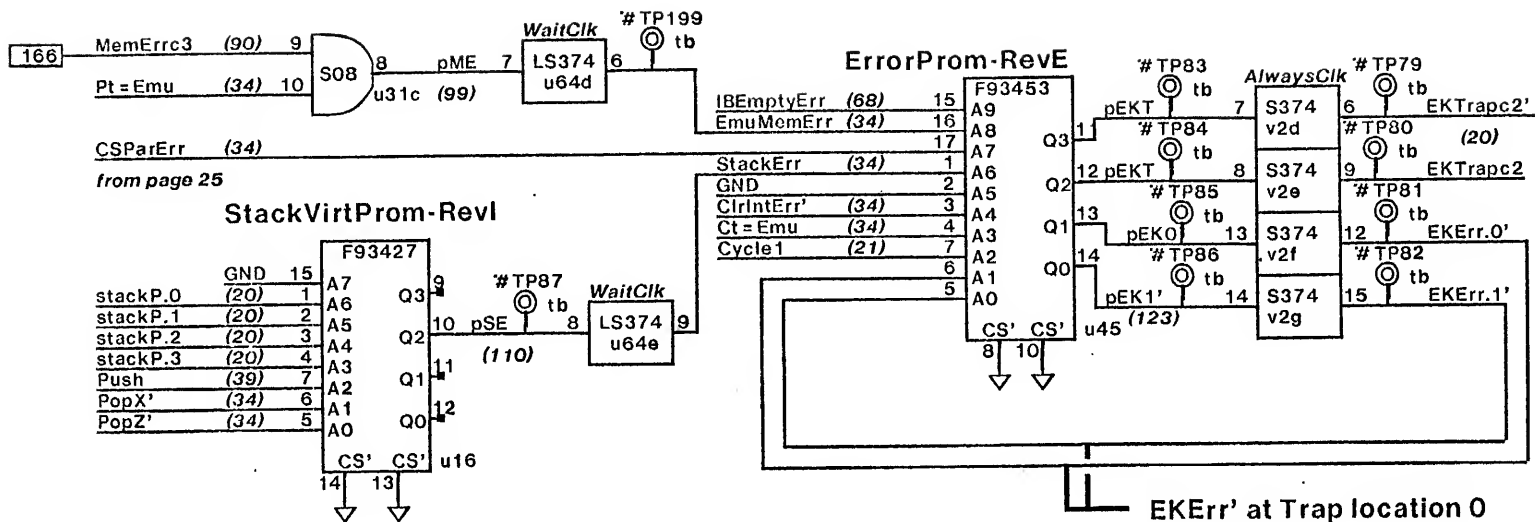
## Click Assignment

0	Ethernet
1	Disk
2	IOP
3	Ethernet/Disk
4	Display/LSEP/Rfrsh

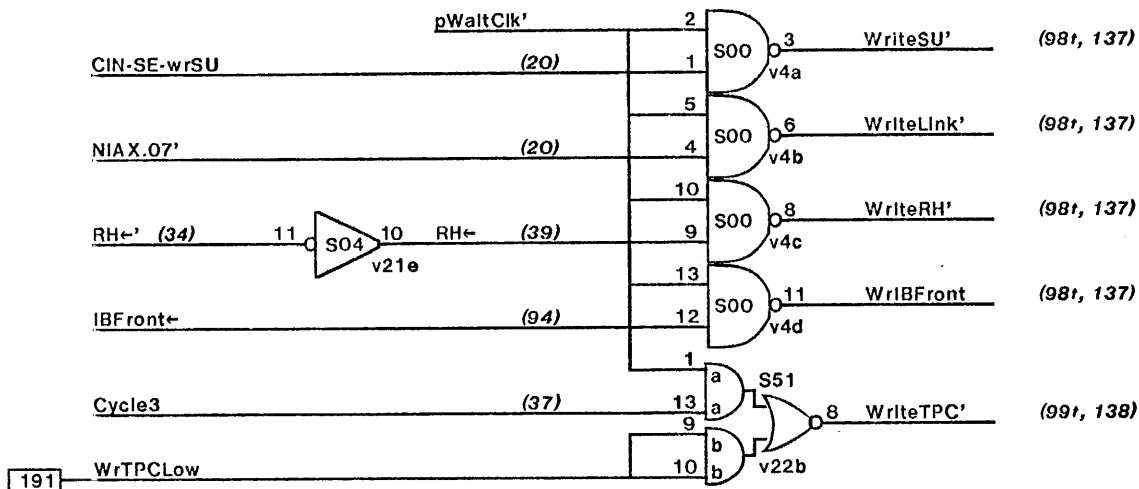
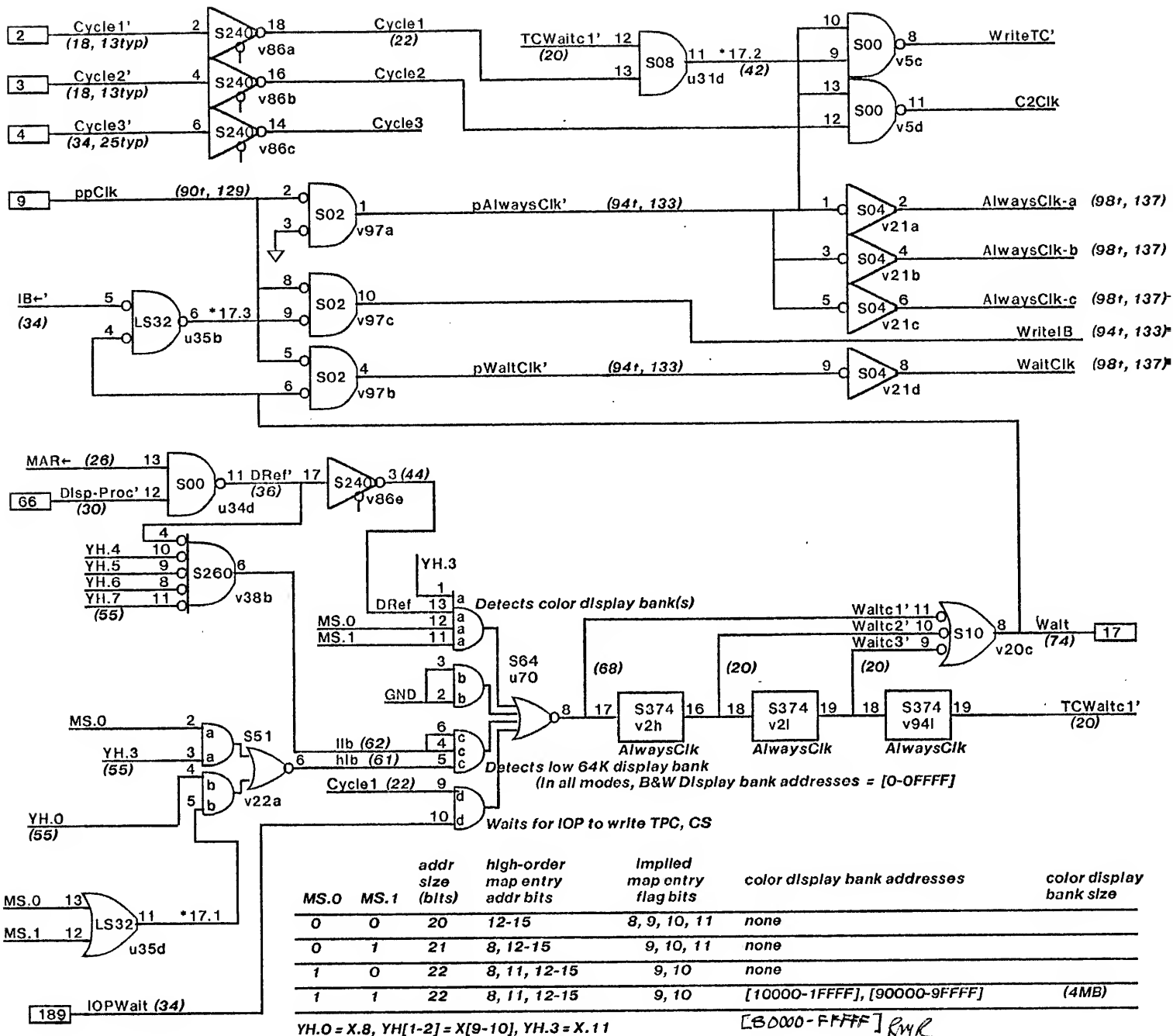
## Notes:

- When Disk = SA4000, Click 3 is Ethernet only.
- When Disk = Trident, Click 3 is Ethernet on even rounds, Trident on Odd rounds (ie, 10-click round)
- The Display & LSEP-refresh tasks never both use Click 4

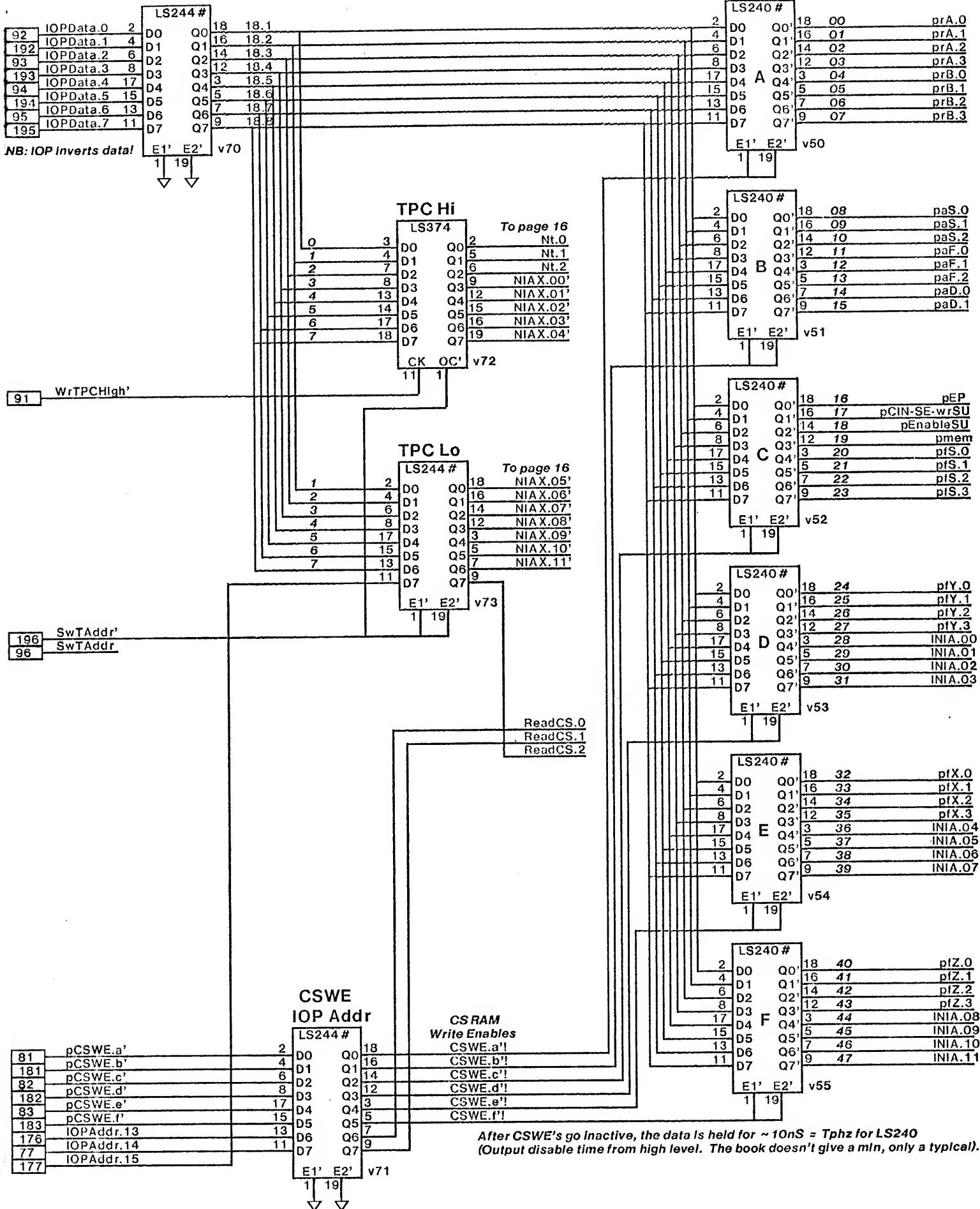
Warning: This drawing contains font 4 macros!

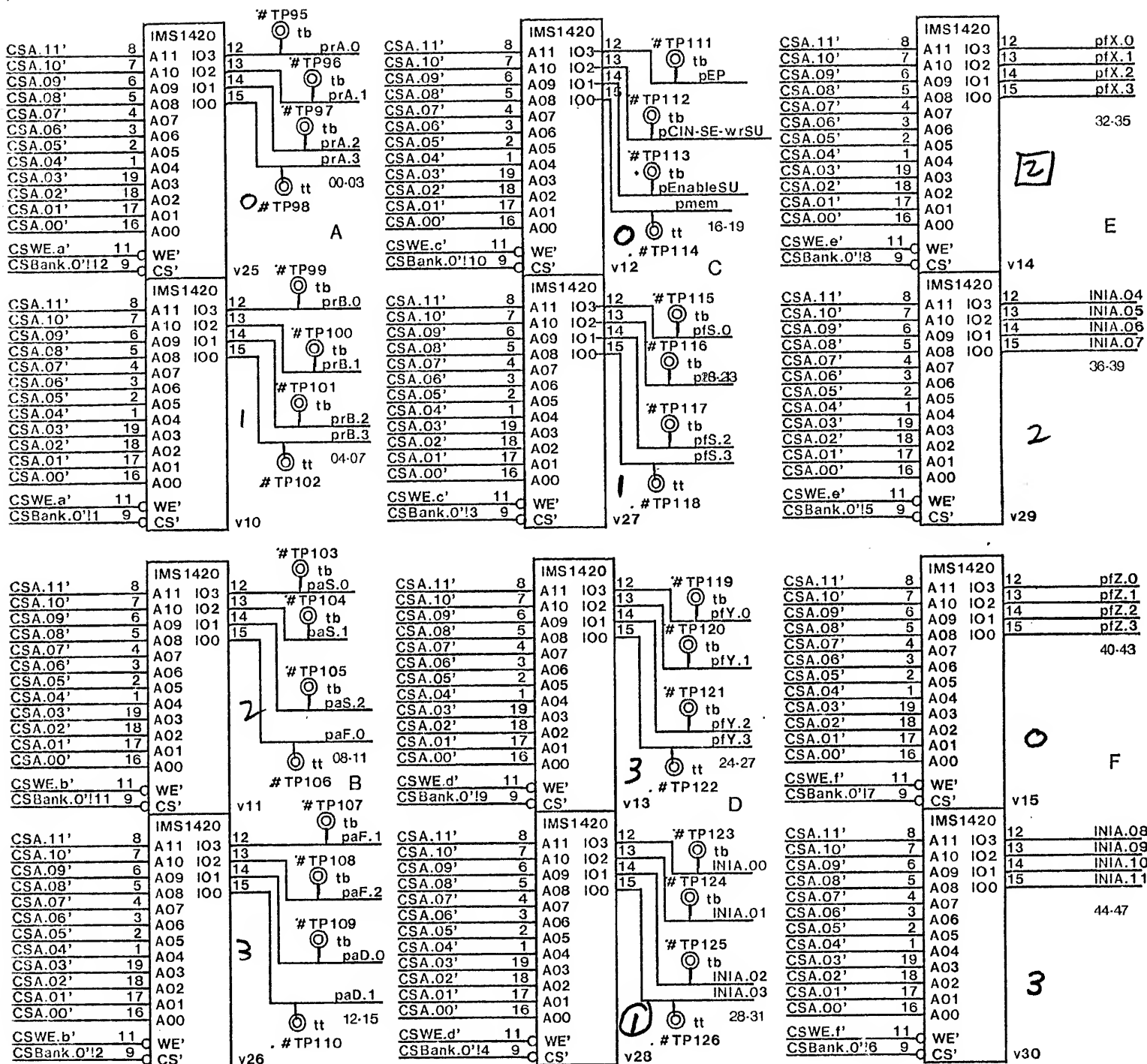


0	IB Empty
1	Stack
2	Emulator Memory
3	CS Parity









0123

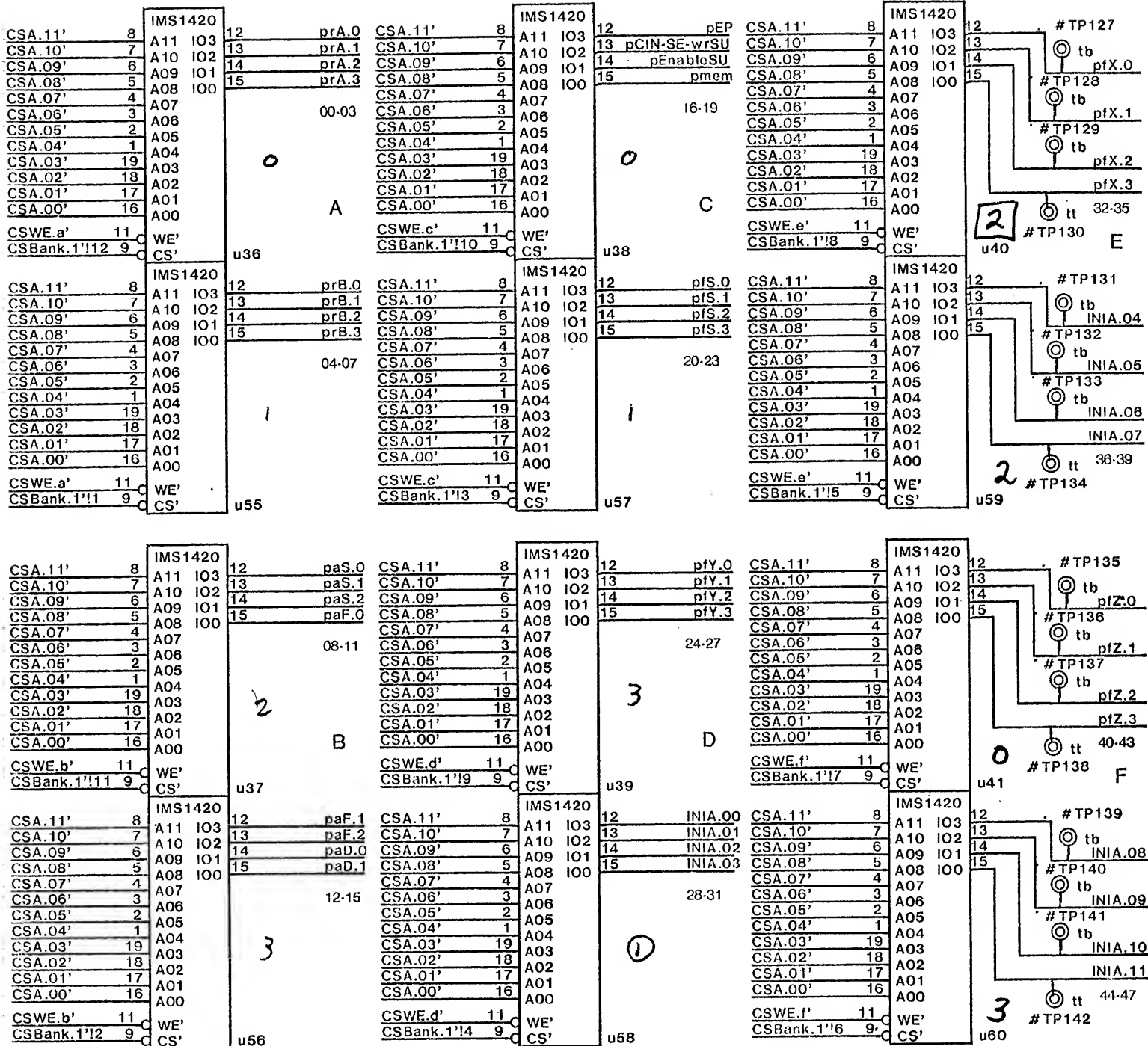
0123

0023

READ		WRITE - Data Hold	
Clock to CSA' valid	17	tPLH for LS240	12
Transmission Delay	13	tPZ for LS244	10
tAA for IMS 1420-55	50		
CS Data valid at	80		22

This suggests that IMS 1420-70 would also work without any trouble.

Warning: This drawing contains font 4 macros!



0123

0123

0023

Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS TITLE SCHEMATIC CDE.FD	DWG SIZE A4	DWG NO. 156P12560 SHEET 21 OF	SHEET REV. A
-------	---	----------------	----------------------------------	-----------------

CSA.11'	8	IMS1420	12	prA.0
CSA.10'	7	A11 IO3	13	prA.1
CSA.09'	6	A10 IO2	14	prA.2
CSA.08'	5	A09 IO1	15	prA.3
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		00-03
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.a'	11	WE'		
CSBank.2'112	9	CS'	u74	

CSA.11'	8	IMS1420	12	prB.0
CSA.10'	7	A11 IO3	13	prB.1
CSA.09'	6	A10 IO2	14	prB.2
CSA.08'	5	A09 IO1	15	prB.3
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		04-07
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.a'	11	WE'		
CSBank.2'11	9	CS'	u92	

CSA.11'	8	IMS1420	12	pEP
CSA.10'	7	A11 IO3	13	pCIN-SE-wrSU
CSA.09'	6	A10 IO2	14	pEnableSU
CSA.08'	5	A09 IO1	15	pmem
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		16-19
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.c'	11	WE'		
CSBank.2'110	9	CS'	u76	

CSA.11'	8	IMS1420	12	pfS.0
CSA.10'	7	A11 IO3	13	pfS.1
CSA.09'	6	A10 IO2	14	pfS.2
CSA.08'	5	A09 IO1	15	pfS.3
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		20-23
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.c'	11	WE'		
CSBank.2'13	9	CS'	u94	

CSA.11'	8	IMS1420	12	pfX.0
CSA.10'	7	A11 IO3	13	pfX.1
CSA.09'	6	A10 IO2	14	pfX.2
CSA.08'	5	A09 IO1	15	pfX.3
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		32-35
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.e'	11	WE'		
CSBank.2'18	9	CS'	u78	

CSA.11'	8	IMS1420	12	INIA.04
CSA.10'	7	A11 IO3	13	INIA.05
CSA.09'	6	A10 IO2	14	INIA.06
CSA.08'	5	A09 IO1	15	INIA.07
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		36-39
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.e'	11	WE'		
CSBank.2'15	9	CS'	u96	

CSA.11'	8	IMS1420	12	paS.0
CSA.10'	7	A11 IO3	13	paS.1
CSA.09'	6	A10 IO2	14	paS.2
CSA.08'	5	A09 IO1	15	paF.0
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		08-11
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.b'	11	WE'		
CSBank.2'111	9	CS'	u75	

CSA.11'	8	IMS1420	12	paF.1
CSA.10'	7	A11 IO3	13	paF.2
CSA.09'	6	A10 IO2	14	paD.0
CSA.08'	5	A09 IO1	15	paD.1
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		12-15
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.b'	11	WE'		
CSBank.2'12	9	CS'	u93	

CSA.11'	8	IMS1420	12	pfY.0
CSA.10'	7	A11 IO3	13	pfY.1
CSA.09'	6	A10 IO2	14	pfY.2
CSA.08'	5	A09 IO1	15	pfY.3
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		24-27
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.d'	11	WE'		
CSBank.2'19	9	CS'	u77	

CSA.11'	8	IMS1420	12	INIA.00
CSA.10'	7	A11 IO3	13	INIA.01
CSA.09'	6	A10 IO2	14	INIA.02
CSA.08'	5	A09 IO1	15	INIA.03
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		28-31
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.d'	11	WE'		
CSBank.2'14	9	CS'	u95	

CSA.11'	8	IMS1420	12	pfZ.0
CSA.10'	7	A11 IO3	13	pfZ.1
CSA.09'	6	A10 IO2	14	pfZ.2
CSA.08'	5	A09 IO1	15	pfZ.3
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		40-43
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.f'	11	WE'		
CSBank.2'17	9	CS'	u79	

CSA.11'	8	IMS1420	12	INIA.08
CSA.10'	7	A11 IO3	13	INIA.09
CSA.09'	6	A10 IO2	14	INIA.10
CSA.08'	5	A09 IO1	15	INIA.11
CSA.07'	4	A08 IO0		
CSA.06'	3	A07		44-47
CSA.05'	2	A06		
CSA.04'	1	A05		
CSA.03'	19	A04		
CSA.02'	18	A03		
CSA.01'	17	A02		
CSA.00'	16	A01		
		A00		
CSWE.f'	11	WE'		
CSBank.2'16	9	CS'	u97	

0123

0123

0023

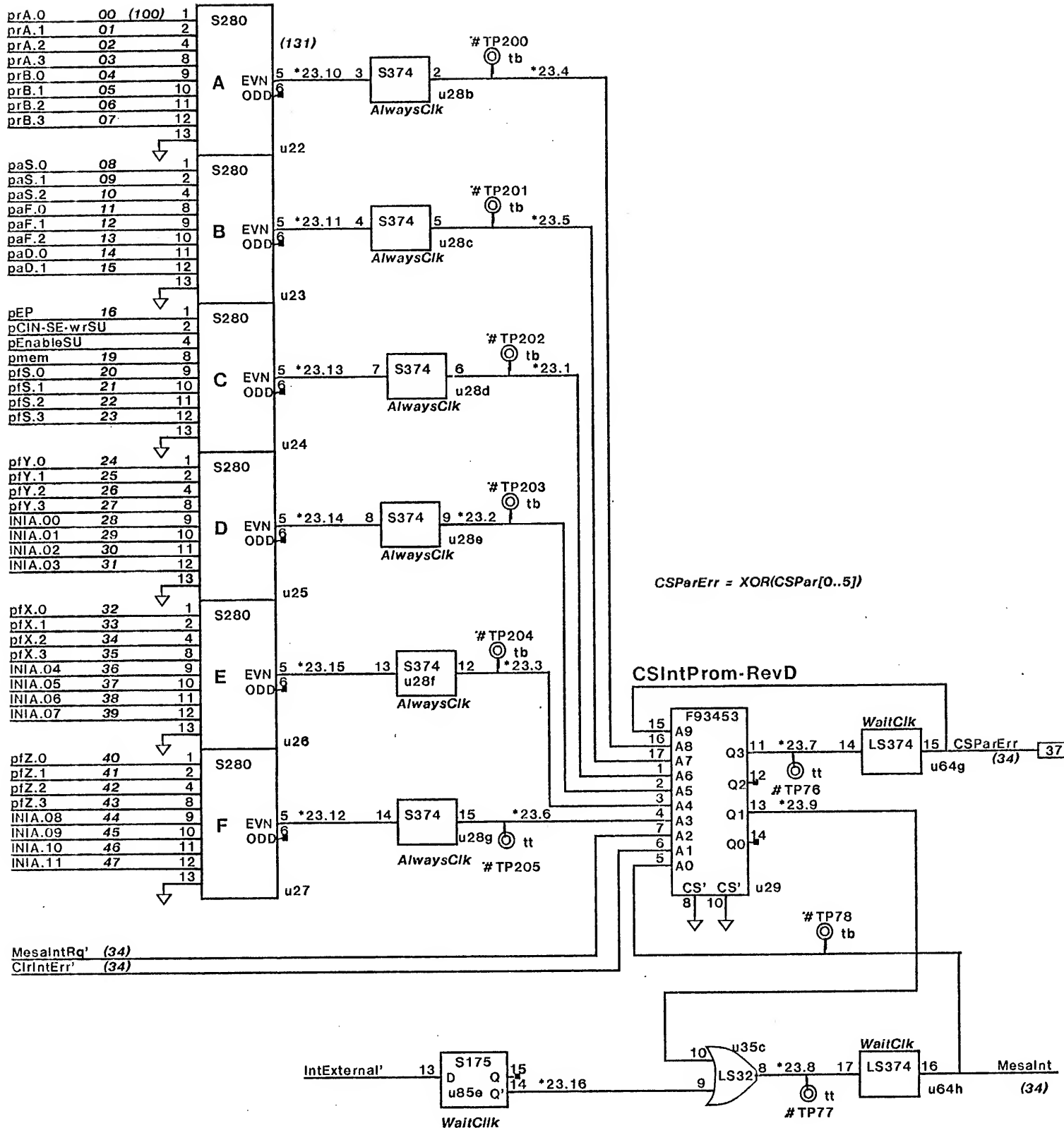
Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC CPE-EP	A4	SHEET 22 OF	A

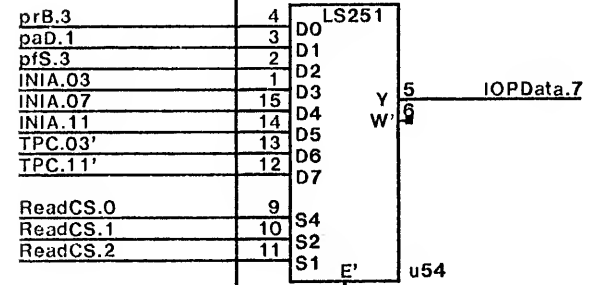
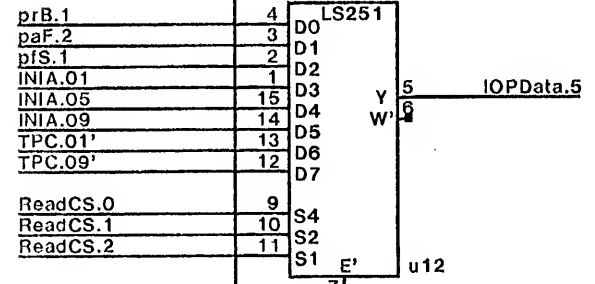
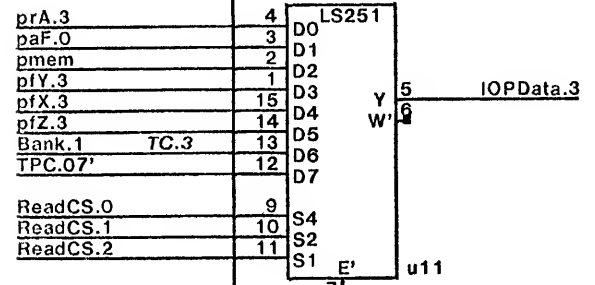
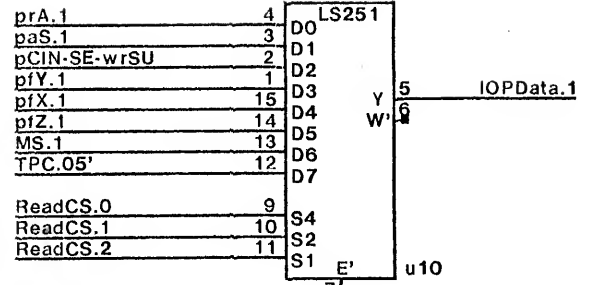
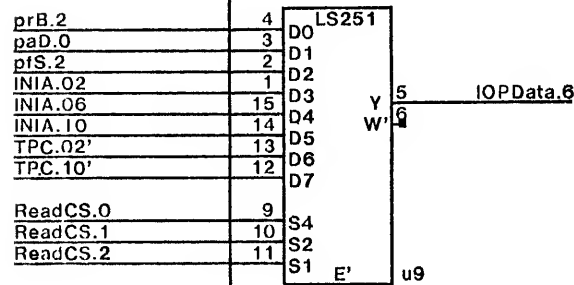
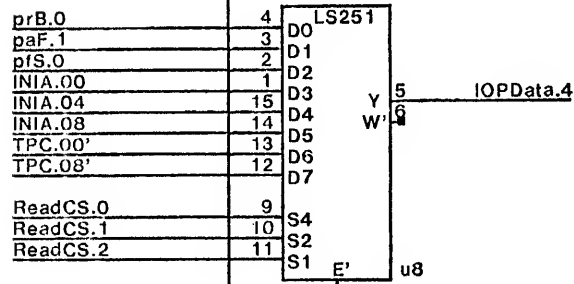
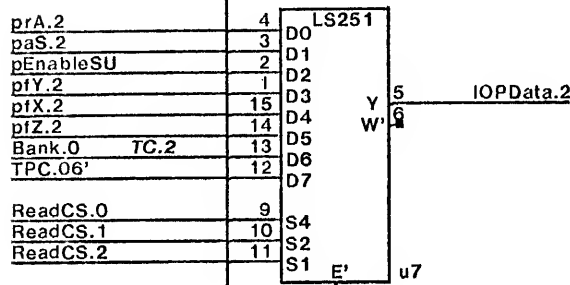
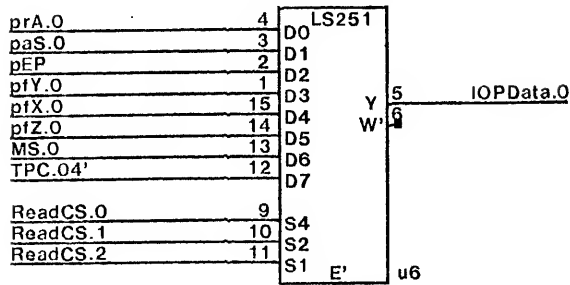
The control Store has been removed to make room for  
the floating point module.

Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P12560		SHEET REV. A
	TITLE SCHEMATIC. CPE-FP			SHEET 23 OF		



NB: TC[0-3] have been replaced by Bank[0-3].



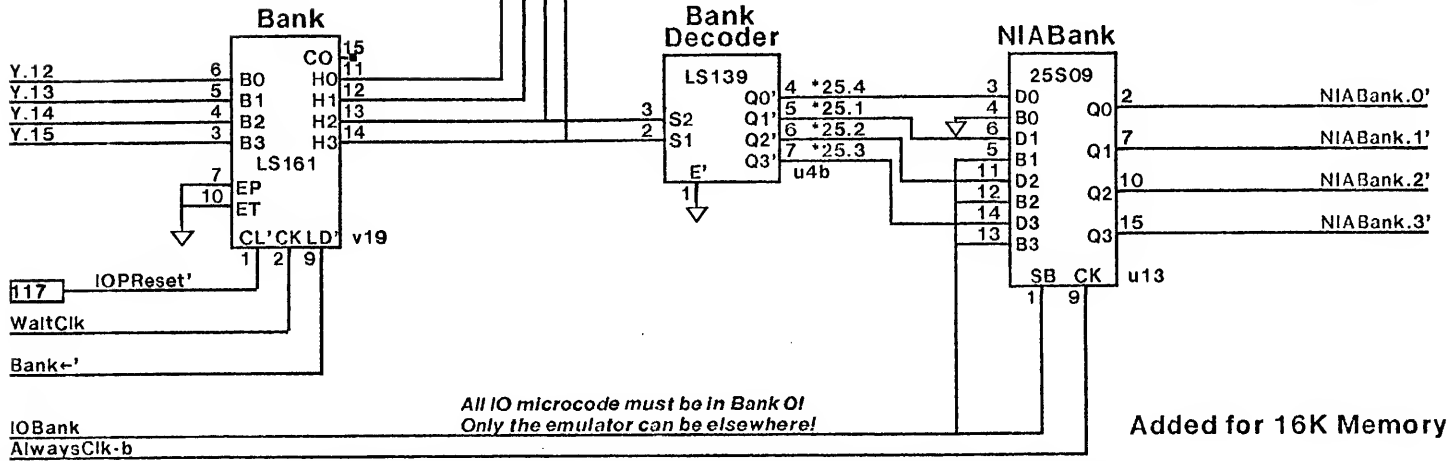
188

ReadCSEn'

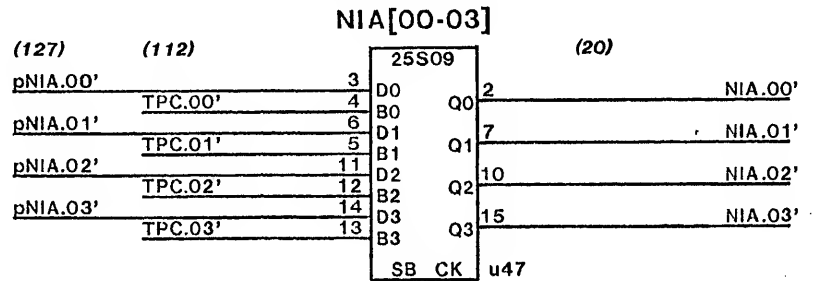
see p. 19

MS.0  
MS.1  
Bank.0  
Bank.1

to p. 26



This section is standard



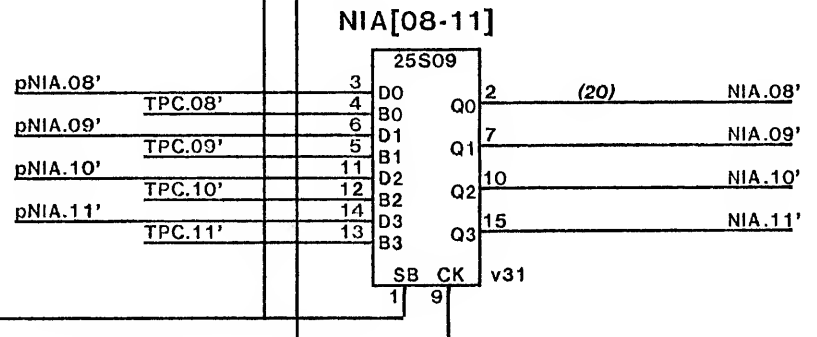
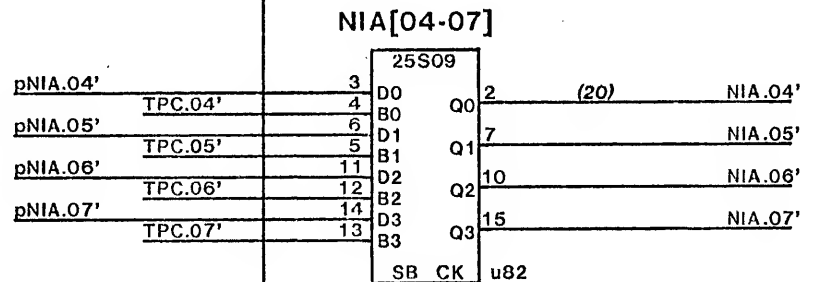
### NOTE on Control Store Addresses

The next instruction address for the control store comes from one of two basic places:

1. TPC registers if switching tasks
2. From the INIA field of the previous microinstruction

In the case of (1), task 6's TPC registers are used by the IOP to provide the address when the IOP wants to read or write data into the control store.

In the case of (2), the INIA field is suitably modified by the trap and conditional branch logic on page 16



Swc2 (122)  
AlwaysClk-c

XEROX

PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS

TITLE SCHEMATIC, CPE-FP

DWG  
SIZE  
A4

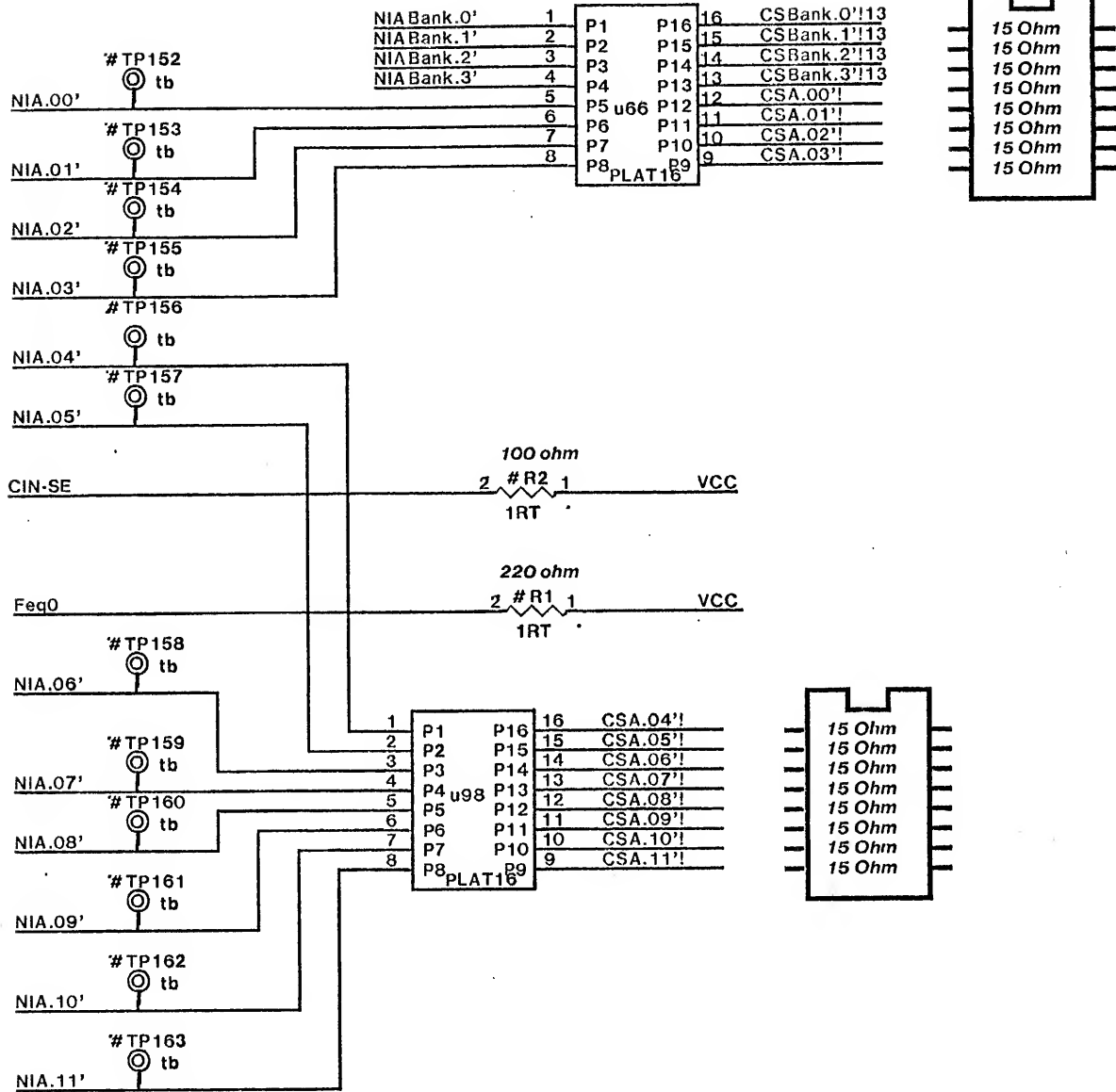
DWG NO. 156P12560

SHEET 26 OF

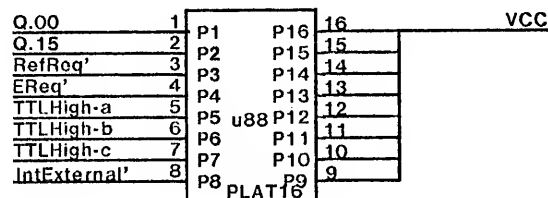
SHEET  
REV.  
A



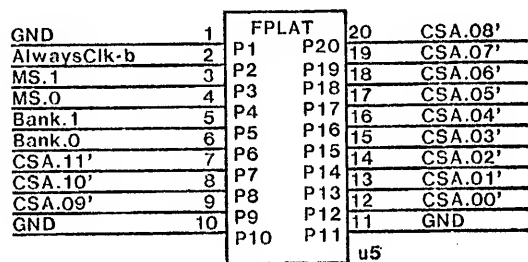
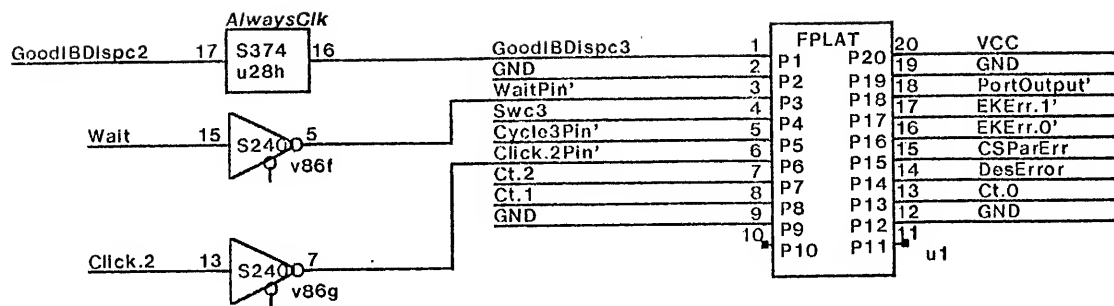
# CS NIA Line Matching



## 1 KOhm Pullups



Beckman Resnet DIP  
898-1-1K

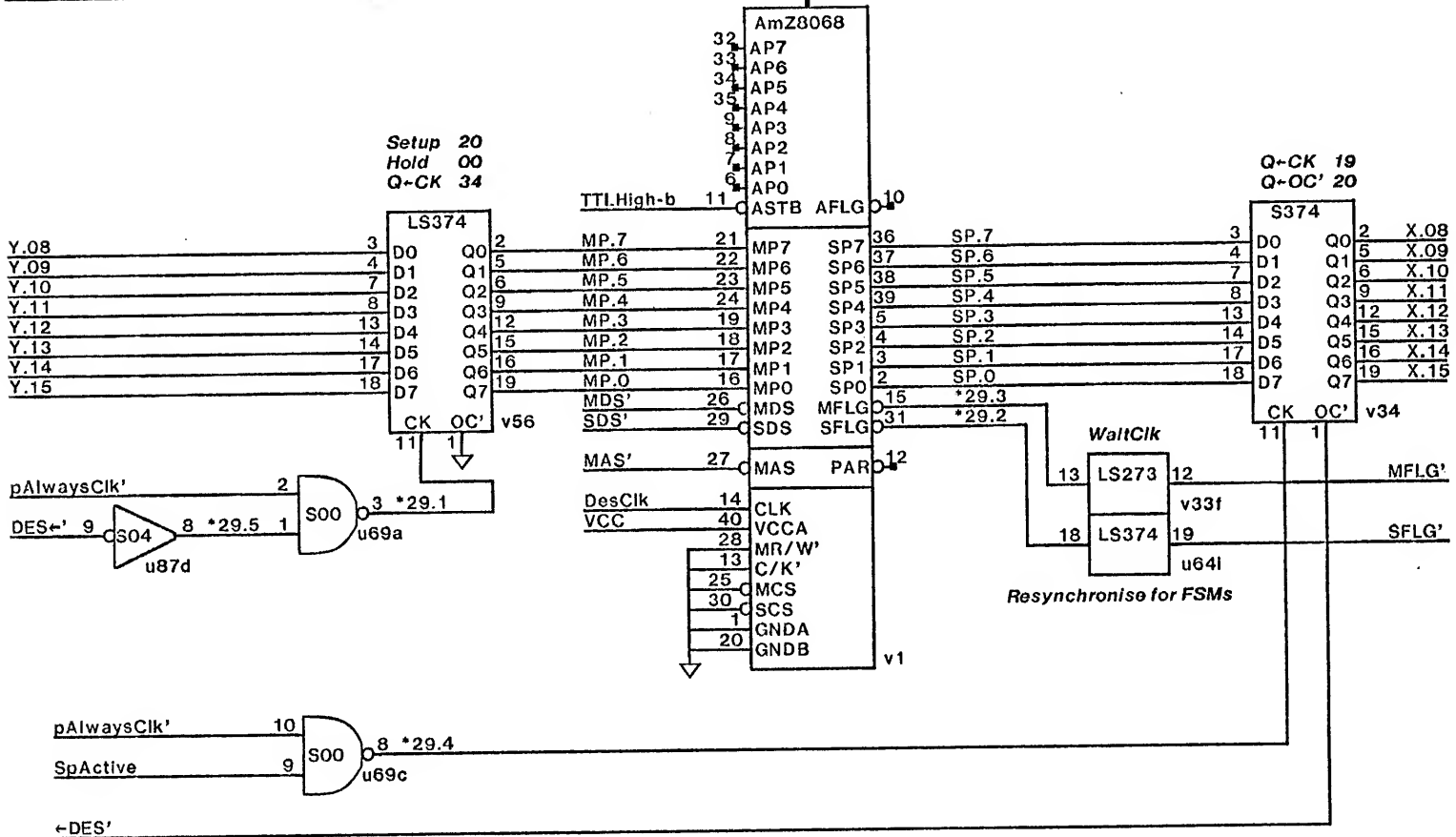


<div>LS374u89</div> <div><div><div>bIBPtr.0</div><div>cIBPtr.1</div><div>dEmuMemErr</div><div>eStackErr</div><div>fpc16'</div><div>gCSParErr</div><div>hMesalnt</div><div>iSFLG'</div></div><div><div><div>LS374u64j</div><div>CKOC</div></div><div>111</div><div>WaitClk</div></div></div>	<div>S374v03</div> <div><div><div>bCSPar.0</div><div>cCSPar.1</div><div>dCSPar.2</div><div>eCSPar.3</div><div>fCSPar.4</div><div>gCSPar.5</div><div>hGoodIBDispc3</div><div>i</div></div><div><div><div>S374u28j</div><div>CKOC</div></div><div>111</div><div>AlwaysClk-b</div></div><div><div><div>S374u28i</div><div>1819</div></div></div></div>	
<div>S374v15</div> <div><div><div>bMAR~'</div><div>cAllowMDR~</div><div>dTC.0</div><div>eTC.1</div><div>fTC.2</div><div>gTC.3</div><div>hKernReq'</div><div>iTCWaitc1'</div></div><div><div><div>S374v94j</div><div>CKOC</div></div><div>111</div><div>AlwaysClk-c</div></div></div>	<div>S374u69</div> <div><div><div>bSwc3~</div><div>cSwc3'</div><div>dEKTrapc2'</div><div>eEKTrapc2</div><div>fEKErr.0'</div><div>gEKErr.1'</div><div>hWaitc2'</div><div>iWaitc3'</div></div><div><div><div>S374v2j</div><div>CKOC</div></div><div>111</div><div>AlwaysClk-a</div></div></div>	
<div>S240w05</div> <div><div><div>aCycle1</div><div>bCycle2</div><div>cCycle3</div><div>dCycle3'</div><div>eDRef</div><div>fWaitPln'</div><div>gClick.2Pln'</div><div>h</div></div><div><div><div>S240v86h</div><div>119</div></div><div><div><div>S240v86i</div><div>EN'</div></div><div>11</div></div><div><div><div>S240v86j</div><div>EN'</div></div><div>19</div></div></div></div> <td><div>S04v43</div><div><div><div>aAD.0'</div><div>bMAR~</div><div>cIBEmptyErr'</div><div>dDes~YBus</div><div>eXBus~SU</div><div>fPort~</div></div></div></td>	<div>S04v43</div> <div><div><div>aAD.0'</div><div>bMAR~</div><div>cIBEmptyErr'</div><div>dDes~YBus</div><div>eXBus~SU</div><div>fPort~</div></div></div>	
<div>S04v39</div> <div><div><div>aAlwaysClk-a</div><div>bAlwaysClk-b</div><div>cAlwaysClk-c</div><div>dWaitClk</div><div>eRH~</div><div>fFne0</div></div></div>	<div>S10x01</div> <div><div><div>aFPCLK</div><div>b~FP'</div><div>cXhigh~0</div></div></div>	<div>S175u35.</div> <div><div><div>bMAS'</div><div>cMDS'</div><div>dSDS'</div><div>eIntExternal</div><div>f*anon*</div></div></div>
<div>S00v42</div> <div><div><div>aXBus~SU'</div><div>bpMAR~'</div><div>cMarPgCross'</div><div>dCIN~pc16</div></div></div>	<div>S00v85</div> <div><div><div>aPop</div><div>bNibble'</div><div>cByte'</div><div>dDRef'</div></div></div>	<div>S00u36</div> <div><div><div>a*anon*</div><div>bWPort</div><div>c*anon*</div><div>dDesClkDisable</div></div></div>
<div>S00v93</div> <div><div><div>aWriteSU'</div><div>bWriteLink'</div><div>cWriteRH'</div><div>dWrIBFront</div></div></div>	<div>S00u33</div> <div><div><div>aPTC.0</div><div>bPTC.1</div><div>cWriteTC'</div><div>dC2Clk</div></div></div>	<div>S00u54</div> <div><div><div>aPByte'</div><div>bSelFP'</div><div>c</div><div>d</div></div><div><div><div>S00v32c</div><div>1098</div></div><div><div><div>S00v32d</div><div>131211</div></div></div></div></div>
<div>S02v08</div> <div><div><div>aPAlwaysCLK'</div><div>bPWaitCLK'</div><div>cWriteIB</div><div>dNt~Pl</div></div></div>	<div>S08v32</div> <div><div><div>aPaSh.0</div><div>bPAllowMDR~</div><div>cPME</div><div>d*anon*</div></div></div>	<div>S51u90</div> <div><div><div>ahlb</div><div>bWrTPC</div></div></div>
<div>S10v79</div> <div><div><div>aSh</div><div>bPush</div><div>cXByte'</div></div></div>	<div>S10v23</div> <div><div><div>aPTC.2</div><div>bPTC.3</div><div>cWait</div></div></div>	<div>S20</div> <div><div><div>aXBus~IB'</div><div>bEnLRotn'</div></div></div>
<div>LS32v98</div> <div><div><div>aDispBr'</div><div>bEnDispBr.3A'</div><div>cEnDispBr2-3B'</div><div>dEnDispBr0-1'</div></div></div>	<div>LS32v20</div> <div><div><div>aLink.0'</div><div>bLink.1'</div><div>cLink.2'</div><div>dLink.3'</div></div></div>	<div>LS32u18</div> <div><div><div>aPRet'</div><div>b*anon*</div><div>cMesalnt</div><div>dM01</div></div></div>
<div>S38v58</div> <div><div><div>aQ.00</div><div>bQ.15</div><div>cCarryIn</div><div>dCarryIn</div></div></div>	<div>S51u90</div> <div><div><div>aWaitc1'</div><div>bWriteTPC'</div></div></div>	<div>S86v81</div> <div><div><div>aPageCross</div><div>bMapRef</div><div>cRefresh</div><div>d</div></div><div><div><div>S86u50d</div><div>131211</div></div></div></div>
<div>S260w04</div> <div><div><div>aIBEmptyErr</div><div>b*anon*</div></div></div>	<div>LS139v49</div> <div><div><div>a8-bit port</div><div>bbank decode</div></div></div>	

## DES Hardware Configuration Information

The chip is hard-wired in multiplexed control mode.  
The Master port is wired for writes only.  
The Auxiliary port is not used at all.  
Data always flows from the Master port to the Slave port.  
Des clock is high for c2 and c3, low for c1  
The microcode is synchronous, so MFLG' is ignored.  
Key parity errors, PAR', are ignored!

Zero out the high X bus when reading DES  
~DES' triggers Xhigh=0 page12(CPE11.sil)

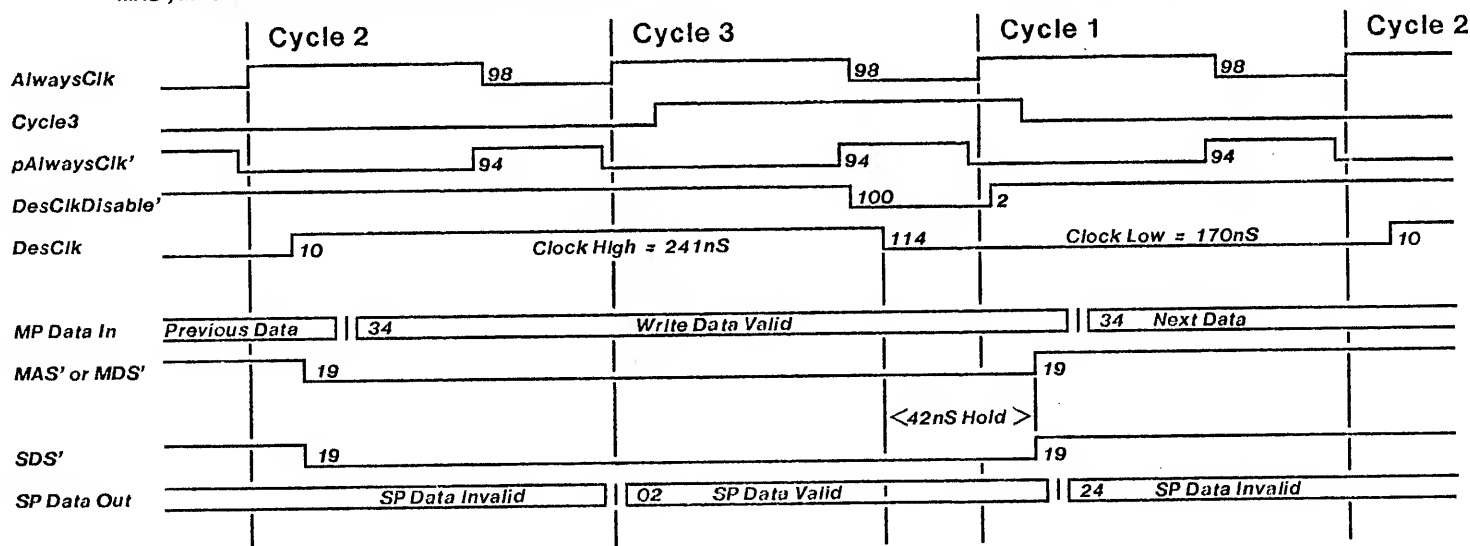


Warning: This drawing contains font 4 macros!

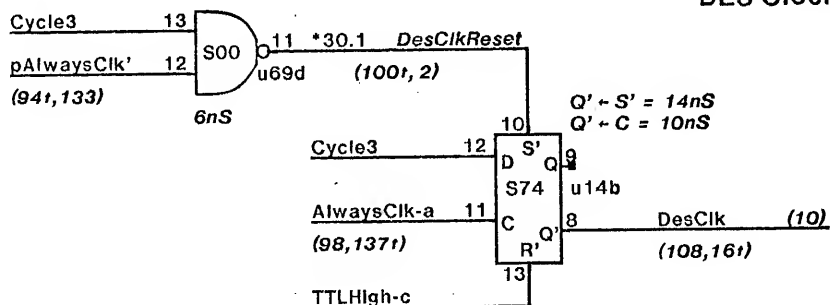
Clock & Reset		AMD #	min.	max.	actual used	Notes
Clock width HIGH		1	115		241	
Clock width LOW		2	115		170	
Clock Cycle		3	250		411	
Clock High to MAS'&MDS' High	Reset Hold	6	0	50	19	
MP and SP Strobe Times						
MAS' falling to MAS' rising (address)	MAS width Low	32	80		274	
MDS' falling to MDS' rising (data)	MDS width Low	44a	125	1000	274	Can't exceed 1000, so have to watch out for WaitClk
MDS' rising to MDS' falling	MDS Recovery	46	125		137	
SDS' falling to SDS' rising (data read)	SDS width Low	44a	125	1000	274	Can't exceed 1000, so have to watch out for WaitClk
SDS' rising to SDS' falling	SDS Recovery	46	125		137	
Clk falling to MDS' rising	MDS Hold	45	20	70	42	This is the difficult bit! See circuitry below.
Clk falling to SDS' rising	SDS Hold	46	20	70	42	This is the difficult bit! See circuitry below.
MAS Write into Master Port						
Data Valid to MAS' rising	Address Setup	36	55		268	
Data Hold after MAS' rising	Address Hold	37	60		243	
MDS Write into Master Port						
Data Valid to MDS' rising	Data Setup	47b	125		268	
Data Hold after MDS' rising	Data Hold	48	80		243	
SDS Read from Slave Port						
SDS falling to Data Valid	SP Access	49b		120		
SDS rising to Data Invalid	SP Data Hold	50	5			
SDS falling to SFLG rising	SP Flag	51		125		for last byte read

### DES Clock Generator Timing

Note: Because of the requirement to hold MDS' and SDS' for 20 to 70 nanoseconds after DesClk falling, we bring DesClk down early in Cycle 3. MAS', MDS' and SDS' follow at the end of Cycle 3.



### DES Clock Generator

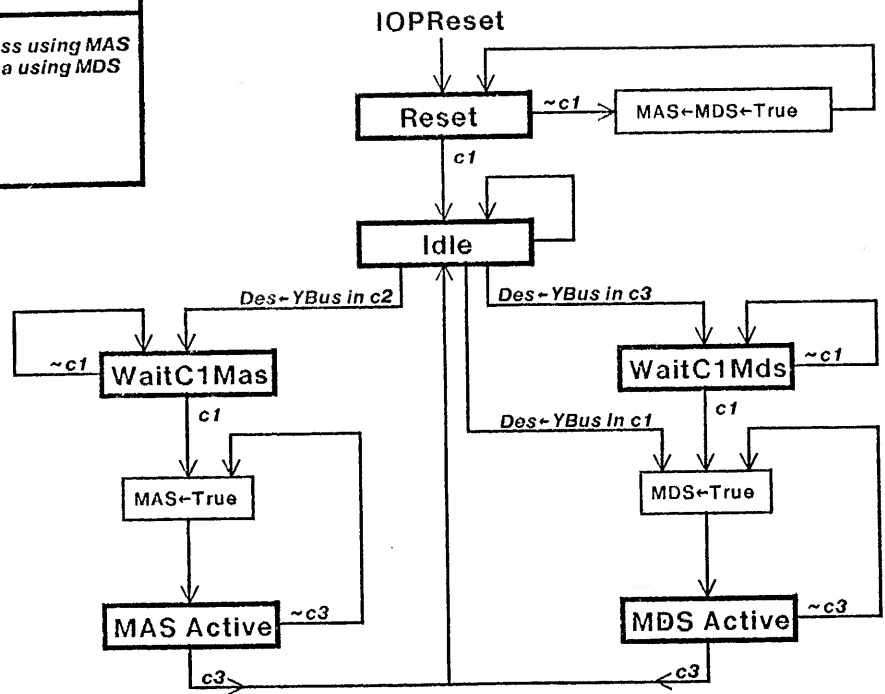




## Note on semantics of Master Port Writes

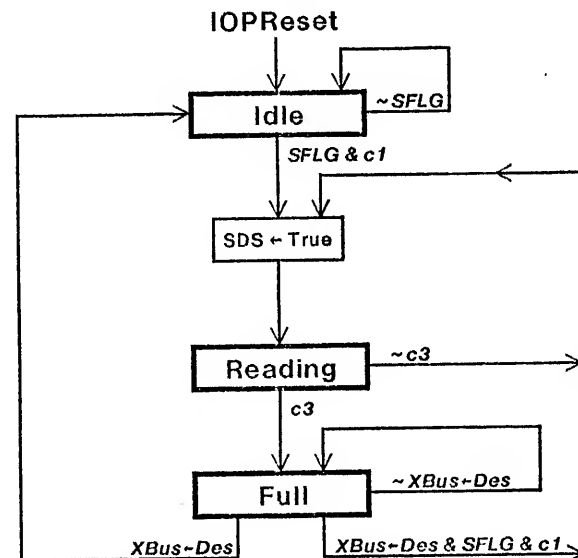
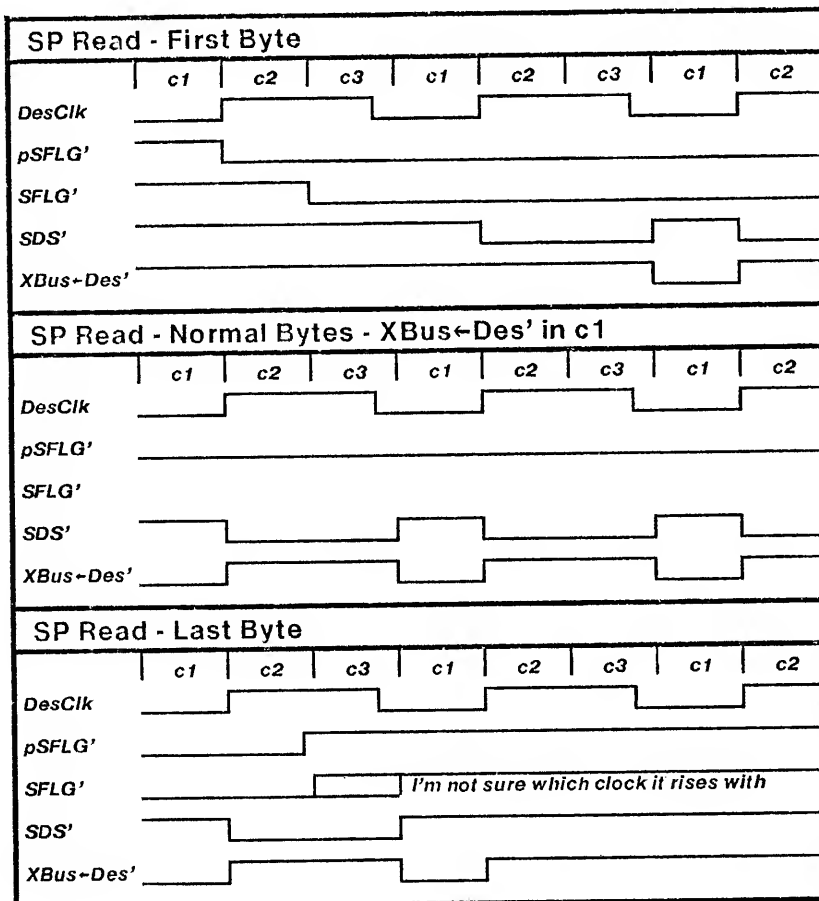
If you write to the Des chip in c2, it means write an address using MAS  
 If you write to the Des chip in c1 or c3, It means write data using MDS  
 You may have to wait for c1 in some of these cases.

The signals are shown logical-true.  
 The implementation below Inverts signals as required.



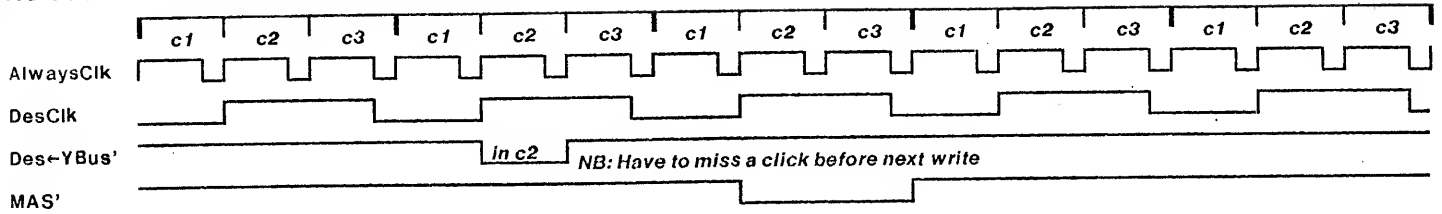
Master Port Finite-State Machine - Error handling of DesMpError signal is not shown

Slave Port Finite-State Machine - Error handling of DesSpError signal is not shown

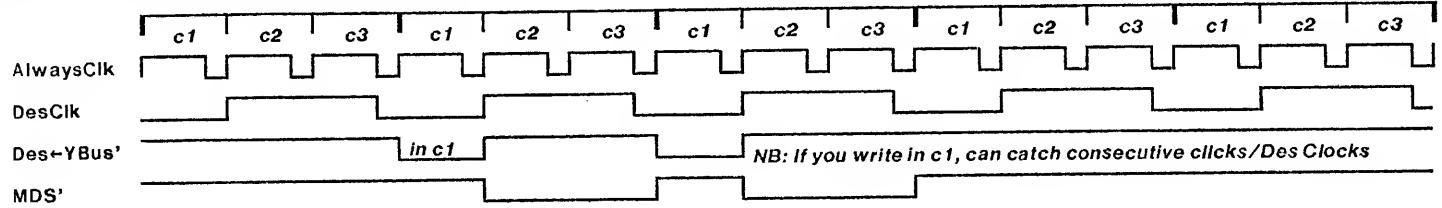


The signals are shown logical-true.  
 The implementation below inverts signals as required.

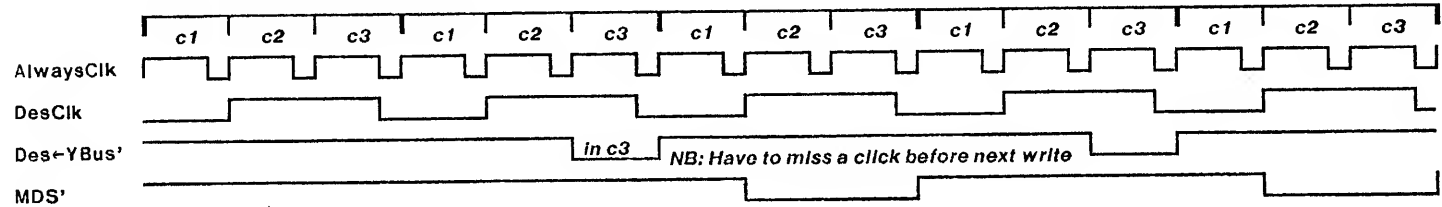
### Write address into Des Master Port in C2



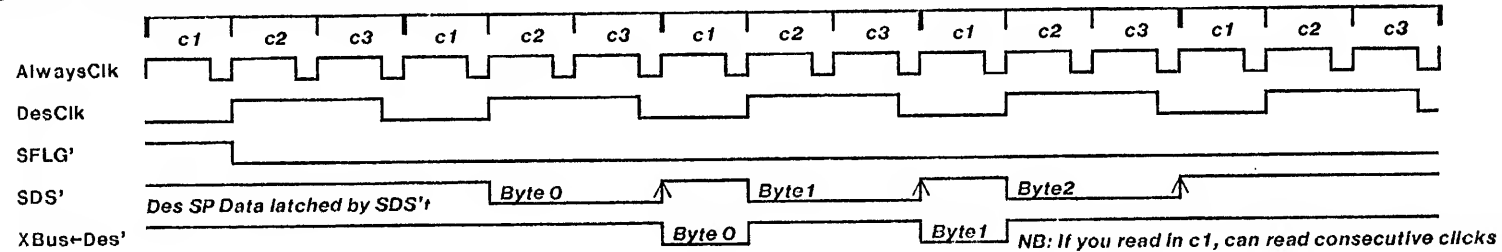
### Write data into Des Master Port in C1



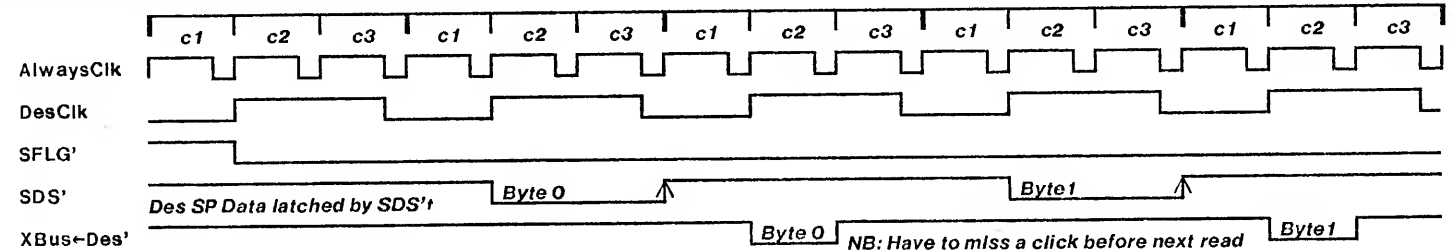
### Write data into Des Master Port in C3



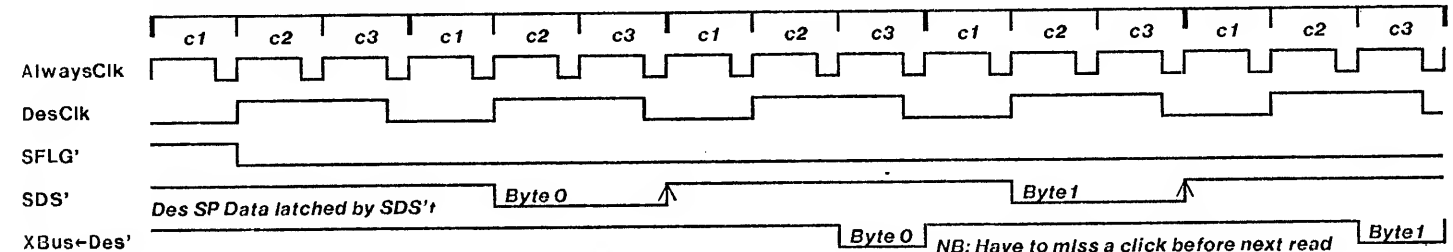
### Read Data from Des Slave Port in C1



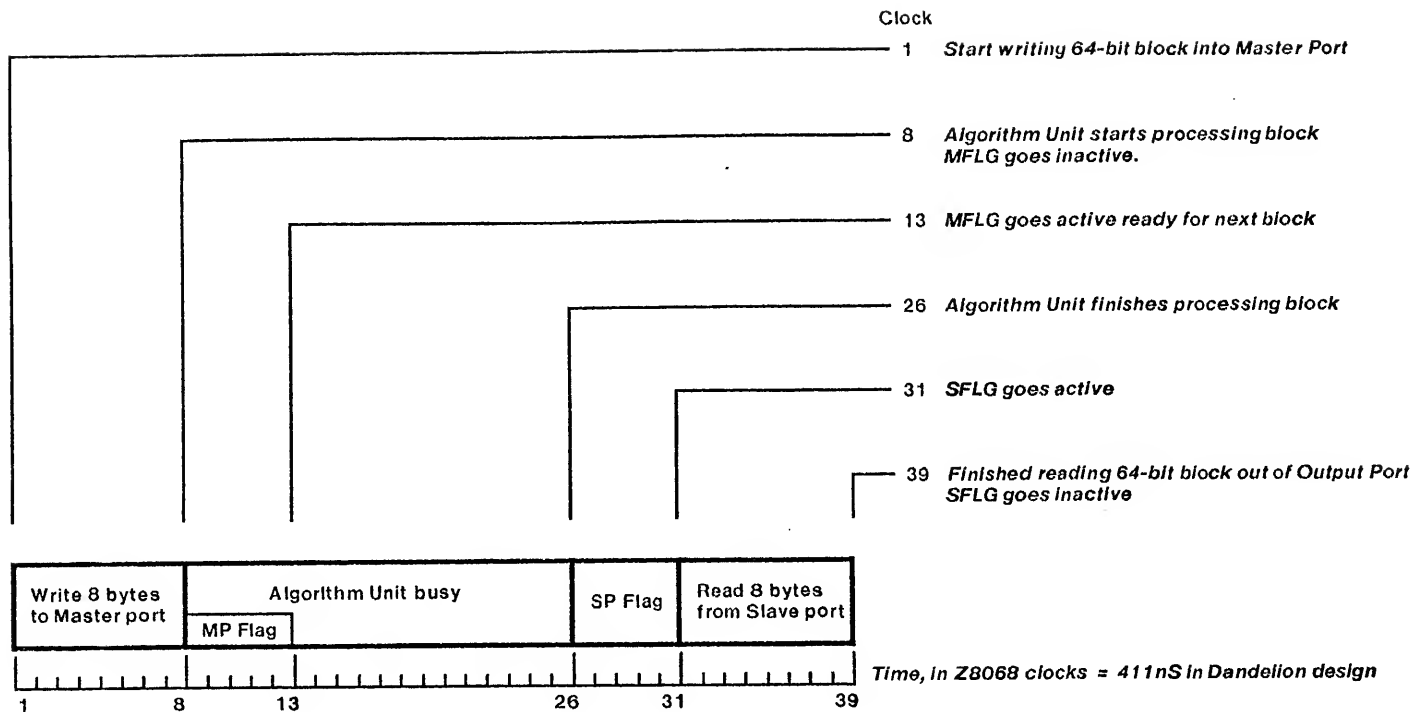
### Read Data from Des Slave Port in C2



### Read Data from Des Slave Port in C3







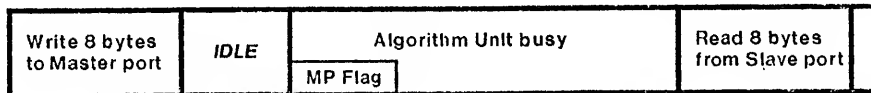
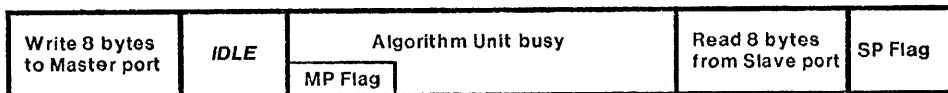
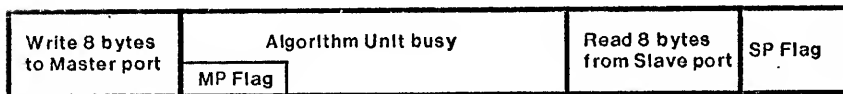
**WARNING! This data is not guaranteed to be correct!**

#### NOTES:

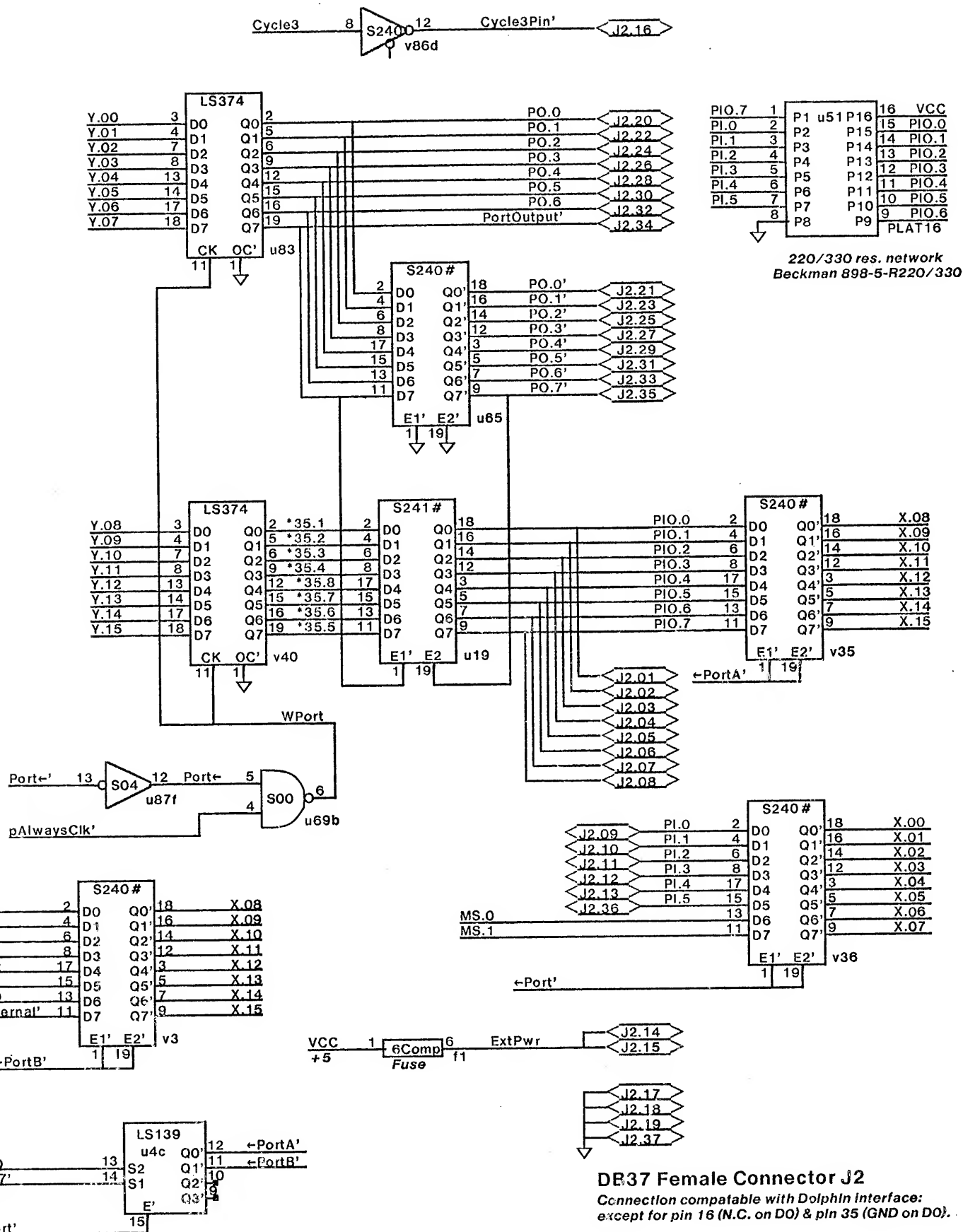
The longest operation in encrypting a block is the time it takes to get the data through the algorithm unit, 18 clocks. Therefore, this is the bottleneck in the pipelining scheme, and the software must aim to keep the Algorithm unit fully busy. Apart from the first and last blocks, the time taken to encrypt the middle blocks is 18 clocks.

#### One possible pipelining scheme

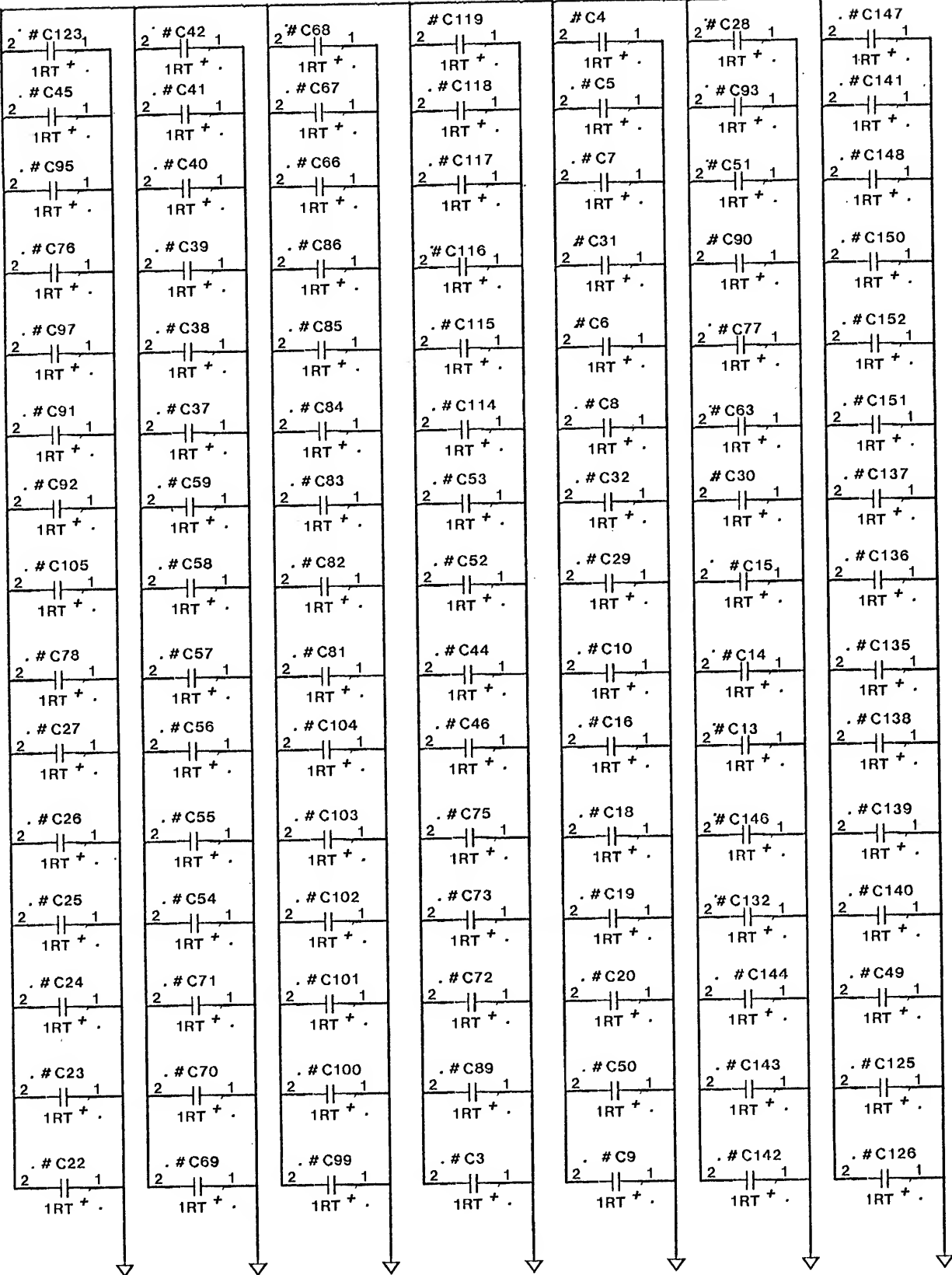
**WARNING! This data is not guaranteed to be correct!**

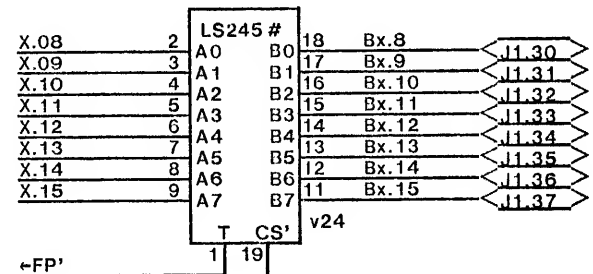
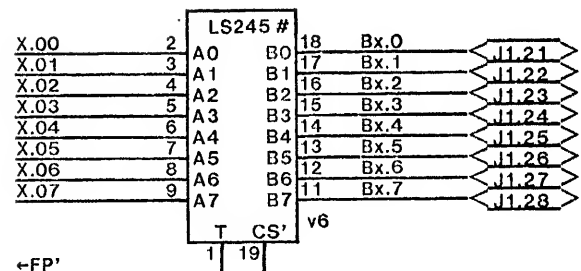
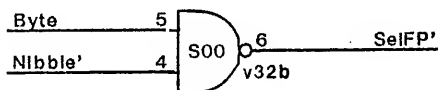
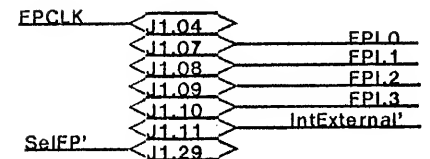
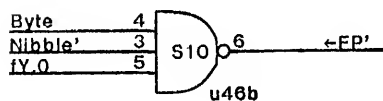
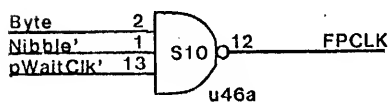
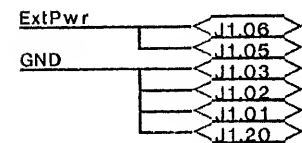
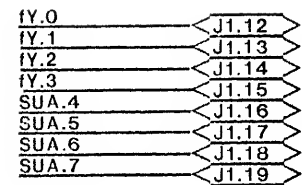
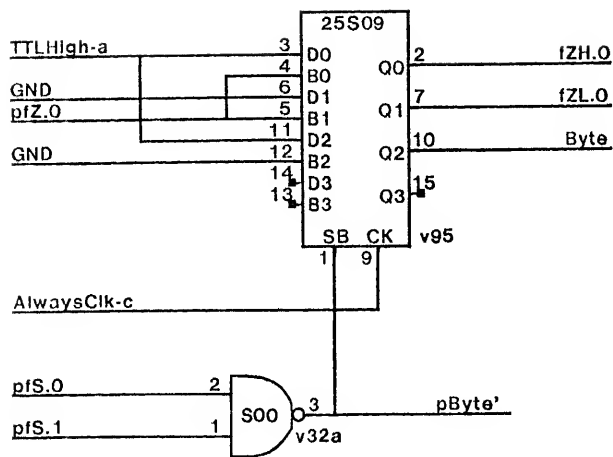


**WARNING! This data is not guaranteed to be correct!**



VCC





DB37 Female Connector J1  
Fast 16-Bit Port

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*Old contents merged with next page*

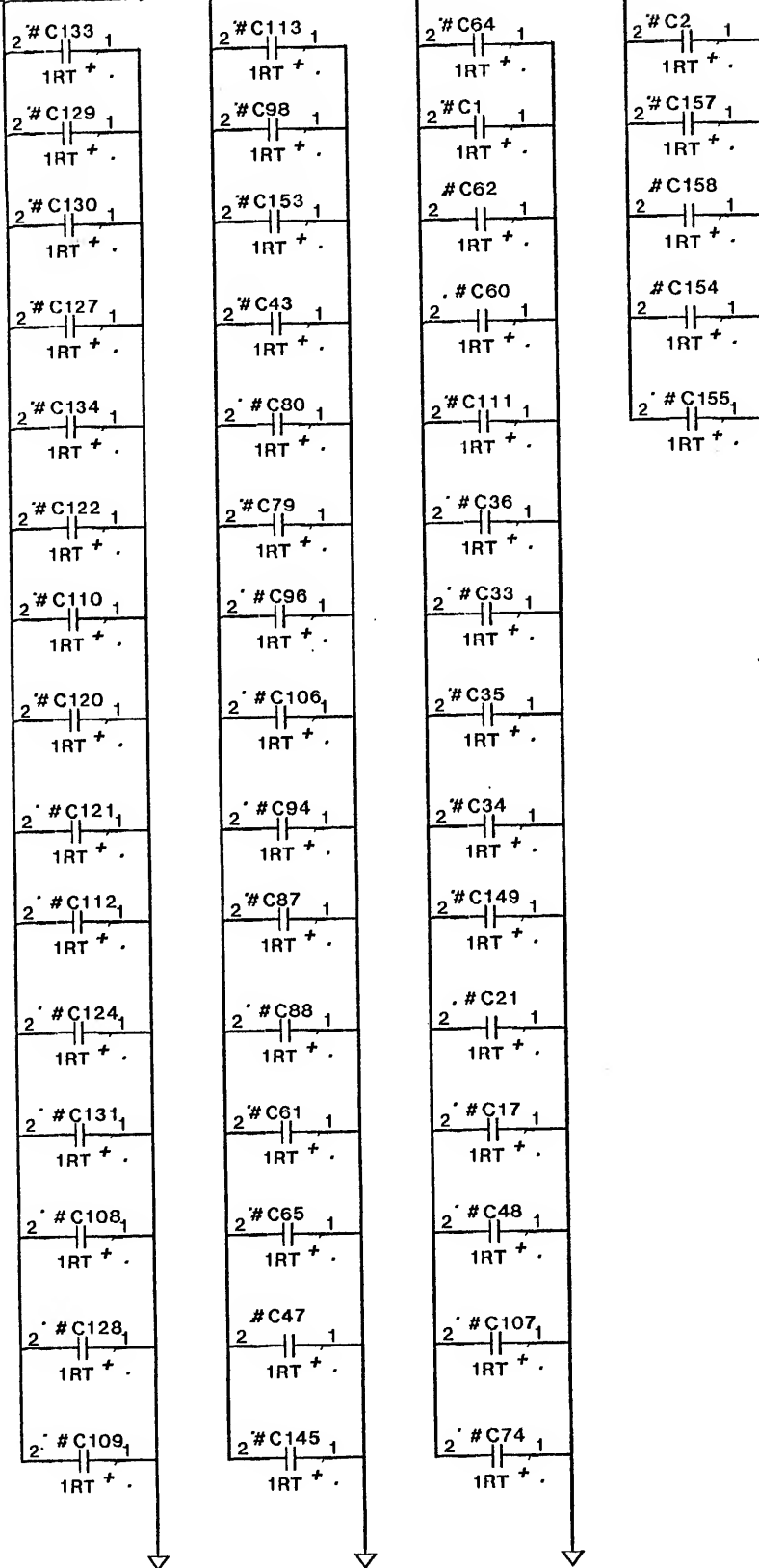
***Floating Point Timing Diagram to be done***

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560		SHEET REV. A
	TITLE SCHEMATIC CRE-ED		SHEET 39	OF	

		PLAT68				
		WTL1032				
FPS.2	1	P1	P68	6	8	GND
Bx.0	2	P2	P67	6	7	FPS.1
Bx.1	3	P3	P66	6	6	FPS.0
Bx.2	4	P4	P65	6	5	Bx.0
Bx.3	5	P5	P64	6	4	Bx.1
Bx.4	6	P6	P63	6	3	Bx.2
Bx.5	7	P7	P62	6	2	Bx.3
Bx.6	8	P8	P61	6	1	Bx.4
Bx.7	9	P9	P60	6	0	Bx.5
Bx.8	10	P10	P59	5	9	Bx.6
Bx.9	11	P11	P58	5	8	VCC
Bx.10	12	P12	P57	5	7	Bx.7
Bx.11	13	P13	P56	5	6	Bx.8
VCC	14	P14	P55	5	5	Bx.9
Bx.12	15	P15	P54	5	4	Bx.10
Bx.13	16	P16	P53	5	3	Bx.11
GND	17	P17	P52	5	2	Bx.12
Bx.14	18	P18	P51	5	1	GND
Bx.15	19	P19	P50	5	0	Bx.13
Bx.0	20	P20	P49	4	9	Bx.14
Bx.1	21	P21	P48	4	8	Bx.15
Bx.2	22	P22	P47	4	7	IY.1
Bx.3	23	P23	P46	4	6	
Bx.4	24	P24	P45	4	5	SUA.7
Bx.5	25	P25	P44	4	4	SUA.6
Bx.6	26	P26	P43	4	3	SUA.5
Bx.7	27	P27	P42	4	2	GND
Bx.8	28	P28	P41	4	1	SUA.4
Bx.9	29	P29	P40	4	0	IY.3
Bx.10	30	P30	P39	3	9	IY.2
Bx.11	31	P31	P38	3	8	Bx.15
Bx.12	32	P32	P37	3	7	VCC
GND	33	P33	P36	3	6	Bx.14
Bx.13	34	P34	P35	3	5	FPCLK

		PLAT68				
		WTL1033				
FPS.2	1	P1	P68	6	8	GND
Bx.0	2	P2	P67	6	7	FPS.1
Bx.1	3	P3	P66	6	6	FPS.0
Bx.2	4	P4	P65	6	5	Bx.0
Bx.3	5	P5	P64	6	4	Bx.1
Bx.4	6	P6	P63	6	3	Bx.2
Bx.5	7	P7	P62	6	2	Bx.3
Bx.6	8	P8	P61	6	1	Bx.4
Bx.7	9	P9	P60	6	0	Bx.5
Bx.8	10	P10	P59	5	9	Bx.6
Bx.9	11	P11	P58	5	8	VCC
Bx.10	12	P12	P57	5	7	Bx.7
Bx.11	13	P13	P56	5	6	Bx.8
VCC	14	P14	P55	5	5	Bx.9
Bx.12	15	P15	P54	5	4	Bx.10
Bx.13	16	P16	P53	5	3	Bx.11
GND	17	P17	P52	5	2	Bx.12
Bx.14	18	P18	P51	5	1	GND
Bx.15	19	P19	P50	5	0	Bx.13
Bx.0	20	P20	P49	4	9	Bx.14
Bx.1	21	P21	P48	4	8	Bx.15
Bx.2	22	P22	P47	4	7	IY.1
Bx.3	23	P23	P46	4	6	
Bx.4	24	P24	P45	4	5	SUA.7
Bx.5	25	P25	P44	4	4	SUA.6
Bx.6	26	P26	P43	4	3	SUA.5
Bx.7	27	P27	P42	4	2	GND
Bx.8	28	P28	P41	4	1	SUA.4
Bx.9	29	P29	P40	4	0	IY.3
Bx.10	30	P30	P39	3	9	IY.2
Bx.11	31	P31	P38	3	8	Bx.15
Bx.12	32	P32	P37	3	7	VCC
GND	33	P33	P36	3	6	Bx.14
Bx.13	34	P34	P35	3	5	FPCLK

VCC



XEROX

PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS

TITLE SCHEMATIC CRE-ED

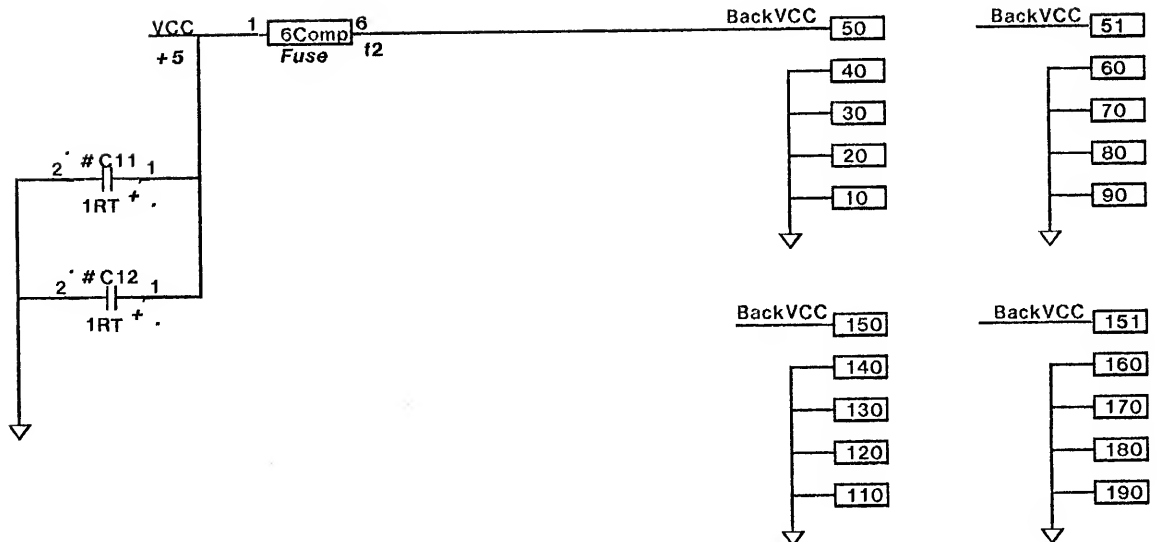
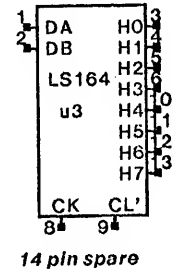
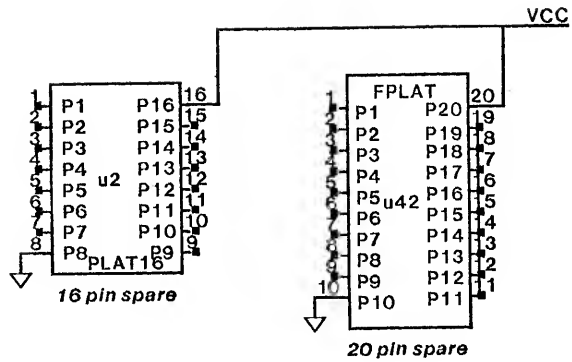
DWG  
SIZE  
A4

DWG NO. 156P12560

SHEET 41 OF

SHEET  
REV.

A





Comments:

- 1) Designator notation notes: u1-99 = U1-99, v0-99 = U100-199, w0-99 = U200-299
- 2) The last item on lines below, preceded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.
- 3) Line with no page number was a continuation of the previous line.

#TP1	.1i	12BitCarry	;04	#TP153	.1i	NIA.01'	;27
#TP10	.1i	IB.2	;07	#TP154	.1i	NIA.02'	;27
#TP100	.1i	prB.1	;20	#TP155	.1i	NIA.03'	;27
#TP101	.1i	prB.2	;20	#TP156	.1i	NIA.04'	;27
#TP102	.1i	prB.3	;20	#TP157	.1i	NIA.05'	;27
#TP103	.1i	paS.0	;20	#TP158	.1i	NIA.06'	;27
#TP104	.1i	paS.1	;20	#TP159	.1i	NIA.07'	;27
#TP105	.1i	paS.2	;20	#TP16	.1i	IBFront←	;07
#TP106	.1i	paF.0	;20	#TP160	.1i	NIA.08'	;27
#TP107	.1i	paF.1	;20	#TP161	.1i	NIA.09'	;27
#TP108	.1i	paF.2	;20	#TP162	.1i	NIA.10'	;27
#TP109	.1i	paD.0	;20	#TP163	.1i	NIA.11'	;27
#TP11	.1i	IB.3	;07	#TP17	.1i	GoodIBDispc2	;07
#TP110	.1i	paD.1	;20	#TP172	.1i	IBPtr.0	;07
#TP111	.1i	pEP	;20	#TP173	.1i	IBPtr.1	;07
#TP112	.1i	pCIN-SE-wrSU	;20	#TP174	.1i	ExitKernel'	;11
#TP113	.1i	pEnableSU	;20	#TP175	.1i	EnterKernel'	;11
#TP114	.1i	pmem	;20	#TP176	.1i	ClrIntErr'	;11
#TP115	.1i	pfS.0	;20	#TP177	.1i	IBDisp'	;11
#TP116	.1i	pfS.1	;20	#TP178	.1i	MesaIntRq'	;11
#TP117	.1i	pfS.2	;20	#TP179	.1i	IBPtr←1'	;11
#TP118	.1i	pfS.3	;20	#TP18	.1i	RefillIntc2	;07
#TP119	.1i	pfY.0	;20	#TP180	.1i	IBPtr←0'	;11
#TP12	.1i	IB.4	;07	#TP181	.1i	PopZ'	;11
#TP120	.1i	pfY.1	;20	#TP182	.1i	←ib'	;11
#TP121	.1i	pfY.2	;20	#TP19	.1i	SelectIB0'	;07
#TP122	.1i	pfY.3	;20	#TP192	.1i	pPC16'	;17
#TP123	.1i	INIA.00	;20	#TP199	.1i	EmuMemErr	;17
#TP124	.1i	INIA.01	;20	#TP2	.1i	PageCross	;04
#TP125	.1i	INIA.02	;20	#TP20	.1i	pIBPtr.0	;07
#TP126	.1i	INIA.03	;20	#TP200	.1i	*23.4	;24
#TP127	.1i	pfX.0	;21	#TP201	.1i	*23.5	;24
#TP128	.1i	pfX.1	;21	#TP202	.1i	*23.1	;24
#TP129	.1i	pfX.2	;21	#TP203	.1i	*23.2	;24
#TP13	.1i	IB.5	;07	#TP204	.1i	*23.3	;24
#TP130	.1i	pfX.3	;21	#TP205	.1i	*23.6	;24
#TP131	.1i	INIA.04	;21	#TP21	.1i	pIBPtr.1	;07
#TP132	.1i	INIA.05	;21	#TP22	.1i	SelectIB1'	;07
#TP133	.1i	INIA.06	;21	#TP23	.1i	MAR←'	;10
#TP134	.1i	INIA.07	;21	#TP24	.1i	DispBr.0'	;13
#TP135	.1i	pfZ.0	;21	#TP25	.1i	DispBr.1'	;13
#TP136	.1i	pfZ.1	;21	#TP26	.1i	DispBr.2'	;13
#TP137	.1i	pfZ.2	;21	#TP27	.1i	DispBr.3A'	;13
#TP138	.1i	pfZ.3	;21	#TP28	.1i	DispBr.3B'	;13
#TP139	.1i	INIA.08	;21	#TP29	.1i	pNIA.00'	;14
#TP14	.1i	IB.6	;07	#TP3	.1i	R.00	;04
#TP140	.1i	INIA.09	;21	#TP30	.1i	pNIA.01'	;14
#TP141	.1i	INIA.10	;21	#TP31	.1i	pNIA.02'	;14
#TP142	.1i	INIA.11	;21	#TP32	.1i	pNIA.03'	;14
#TP15	.1i	IB.7	;07	#TP33	.1i	pNIA.04'	;14
#TP152	.1i	NIA.00'	;27	#TP34	.1i	pNIA.05'	;14

#TP35	.1i	pNIA.06'	;14	#TP91	.1i	pKR'	;17
#TP36	.1i	pNIA.07'	;14	#TP93	.1i	KernReq'	;17
#TP37	.1i	ptC.0	;14	#TP94	.1i	pc16'	;17
#TP38	.1i	pNIA.08'	;14	#TP95	.1i	prA.0	;20
#TP39	.1i	ptC.1	;14	#TP96	.1i	prA.1	;20
#TP4	.1i	R.15	;04	#TP97	.1i	prA.2	;20
#TP40	.1i	pNIA.09'	;14	#TP98	.1i	prA.3	;20
#TP41	.1i	ptC.2	;14	#TP99	.1i	prB.0	;20
#TP42	.1i	pNIA.10'	;14				
#TP43	.1i	ptC.3	;14	E002		Cycle1'	;18
#TP44	.1i	pNIA.11'	;14	E003		Cycle2'	;18
#TP45	.1i	TPC.00'	;15	E004		Cycle3'	;18
#TP46	.1i	TPC.01'	;15	E009		ppClk	;18
#TP47	.1i	TPC.02'	;15	E010		GND	;42
#TP48	.1i	TPC.03'	;15	E011		AllowMDR←	;10
#TP49	.1i	TPC.04'	;15	E015		MapRef	;12
#TP5	.1i	Q.00	;04	E016		Refresh	;12
#TP50	.1i	TPC.05'	;15	E017		Wait	;18
#TP51	.1i	TPC.06'	;15	E020		GND	;42
#TP52	.1i	TPC.07'	;15	E021		IOPData←'	;11
#TP53	.1i	TPC.08'	;15	E022		KOData←'	;11
#TP54	.1i	TPC.09'	;15	E023		EOData←'	;11
#TP55	.1i	TPC.10'	;15	E024		DCtlFifo←'	;11
#TP56	.1i	TPC.11'	;15	E025		DBorder←'	;11
#TP57	.1i	pLink.0'	;15	E026		←TStatus'	;11
#TP58	.1i	pLink.1'	;15	E027		KCmd←'	;11
#TP59	.1i	pLink.2'	;15	E028		POData←'	;11
#TP6	.1i	Q.15	;04	E030		GND	;42
#TP60	.1i	pLink.3'	;15	E031		←EIData'	;11
#TP61	.1i	TCY.0	;15	E032		←KIData'	;11
#TP62	.1i	TCY.1	;15	E033		←KTest'	;11
#TP63	.1i	TCY.2	;15	E034		←IOPIData'	;11
#TP64	.1i	TCY.3	;15	E035		ESTrobe'	;11
#TP65	.1i	Ct.0	;16	E037		CSParErr	;24
#TP66	.1i	Ct.1	;16	E039		YIODisp.0	;13
#TP67	.1i	Ct.2	;16	E040		GND	;42
#TP68	.1i	Ct=Emu	;16	E041		X.00	;03
#TP69	.1i	Pt=Emu	;16	E042		X.02	;03
#TP7	.1i	CIN-SE	;04	E043		X.04	;03
#TP70	.1i	Nt.0	;16	E044		X.06	;03
#TP71	.1i	Nt.1	;16	E045		X.08	;03
#TP72	.1i	Nt.2	;16	E046		X.10	;03
#TP73	.1i	Nt=Emu	;16	E047		X.12	;03
#TP74	.1i	Swc2	;16	E048		X.14	;03
#TP75	.1i	Swc2'	;16	E049		Y.00	;03
#TP76	.1i	*23.7	;24	E050		BackVCC	;42
#TP77	.1i	*23.8	;24	E051		BackVCC	;42
#TP78	.1i	MesaInt	;24	E052		Y.02	;03
#TP79	.1i	EKTrapc2'	;17	E053		Y.04	;03
#TP8	.1i	IB.0	;07	E054		Y.06	;03
#TP80	.1i	EKTrapc2	;17	E055		Y.08	;03
#TP81	.1i	EKErr.0'	;17	E056		Y.10	;03
#TP82	.1i	EKErr.1'	;17	E057		Y.12	;03
#TP83	.1i	pEKT	;17	E058		Y.14	;03
#TP84	.1i	pEKT	;17	E059		YH.0	;06
#TP85	.1i	pEK0'	;17	E060		GND	;42
#TP86	.1i	pEK1'	;17	E061		YH.2	;06
#TP87	.1i	pSE	;17	E062		YH.4	;06
#TP9	.1i	IB.1	;07	E063		YH.6	;06

E064	Pt.0	;16	E155	Y.09	;03
E065	Pt.2	;16	E156	Y.11	;03
E066	Disp-Proc'	;18	E157	Y.13	;03
E070	GND	;42	E158	Y.15	;03
E077	IOPAddr.14	;19	E159	YH.1	;06
E080	GND	;42	E160	GND	;42
E081	pCSWE.a'	;19	E161	YH.3	;06
E082	pCSWE.c'	;19	E162	YH.5	;06
E083	pCSWE.e'	;19	E163	YH.7	;06
E084	IOPReq'	;16	E164	Pt.1	;16
E085	DPReq'	;16	E166	MemErrc3	;17
E086	EReq'	;16	E170	GND	;42
E087	KReq'	;16	E176	IOPAddr.13	;19
E088	RefReq'	;16	E177	IOPAddr.15	;19
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	TITLE	SCHEMATIC CDE EP	A4	SHEET	75 OF	A